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Preliminary Edition

UCT Maintenance Manual

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REMINGTON RAND UNIVAC ®
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Philadelphia, Pa.
July 1958

UCT MAINTENANCE MANUAL

Preliminary Sections

The purpose of the three sections in this manual is to familiarize maintenance personnel with the physical layout and components of the processor, and with the printed maintenance aids which accompany the UCT system. As more detailed maintenance information becomes available, it will be published and forwarded to holders of this manual.

Section 1 contains a physical description of the components used in the processor and the location of each by means of photographs and illustrations. In Section 2, the various types of printed maintenance aids, such as drawings and tables, are described together with the prescribed procedure for their use. Section 3 contains a description of the various controls and indicators on the Operator's and Engineer's Panels in the Processor.

UCT MAINTENANCE MANUAL

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SECTION 2 PRINTED MAINTENANCE AIDS

SECTION 3 CONTROL PANELS

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SECTION ONE

PHYSICAL DESCRIPTION

1.1 GENERAL

The two sections of the UCT Processor are designated as the power supply unit and the package area. The power supply unit contains the power supplies, motors, storage drum, blower system, control panels and other miscellaneous components. The package area consists of two bays, one fixed and one hinged, that contain the printed circuit packages.

The distribution of the power supply voltage to the bays and input-output devices is accomplished by means of barrier strips, connectors, and busbars. However, no set pattern for distribution of power exists, as can be seen in Figure 1-1 which illustrates several of the many variations in the distribution of the power supply voltages.

1.2 POWER SUPPLY UNIT

The power supply unit (Figures 1-2 and 1-3) contains 17 power supply chassis which provide all of the dc voltages for the processor and most of the dc voltages for the input-output units. Figures 1-2 and 1-3 show the physical layout of these chassis. The unit also houses the barrier strips and connectors which distribute the voltages. In later models of the UCT the power supplies are grouped together, as shown in Figures 1-2b and 1-3b, resulting in fewer power supply chassis.

The storage drum, clock chassis, control panels, blower, motors and alternator are all contained within the power supply unit. Each item contained in the power supply unit is shown in Figures 1-2 and 1-3 and explained in the following paragraphs. The control panels are described in section 3.

1.2.1 Power Supply Chassis

The power supply chassis (Figures 1-2 and 1-3) provide the processor with dc voltage. Each power supply chassis has a barrier strip attached to it to serve as a distribution point. A barrier strip consists of a set of terminals on a bakelite board. The number of terminals on each barrier strip varies from 2 to 12. Each chassis is pointed out in Figures 1-2 and 1-3 along with the barrier strip that serves it. The distribution of the power supply voltages is shown in engineering drawings DX805, 632 or DX805, 633 supplied with the system.

1.2.2 Clock Driver Chassis

The clock driver chassis (Figure 1-2a) contains the various components necessary to shape and amplify a sine wave. Test terminals, tuning and control devices are located on the left edge of the chassis (see Figure 1-4). The top edge contains three coax connectors and a 24 terminal connector plug.

The clock driver chassis receives a sine wave from the drum, amplifies and shapes it, and then produces an output which consists of two sine waves equal in amplitude but 180 degrees out of phase. The two sine waves then drive the clock output chassis. A complete circuit analysis of this chassis is contained in section 6 of the UCT Processor Manual. The wiring and circuit schematic of the clock driver chassis are shown in Engineering Drawings DX601, 163 and DX808, 412.

1.2.3 Clock Output Chassis

The clock output chassis (Figure 1-2a) receives as input the two sine wave outputs of the driver chassis. The output chassis receives the two sine waves, increases their power, and produces A and B phase sine waves. A single tuning shaft, for the tank circuit of the output chassis, is on the top edge of the chassis. The output transformer is above the chassis.

The complete circuit analysis of this chassis is contained in section 6 of the Processor Manual. Engineering drawings show the complete circuitry and wiring of the output chassis.

1.2.4 Storage Drum

The storage drum (Figure 1-2a) is sealed in a container located next to the clock driver chassis. The container is filled with helium at a pressure of one third of an atmosphere. The container is bolted to a mounting plate which contains 27 connector plugs set in two circles. The drum-to-processor wiring drawing DX805, 754 shows the drum plate and indicates the use of each connector plug.

1.2.5 Bleeder Resistor and Rectifier Panel

The bleeder resistor and rectifier panel (Figure 1-5) contain resistors, potentiometers, a meter relay (Relay 31), three pyrometers, selenium rectifiers, and mounting boards.

Seven of the bleeder resistors have adjustable sliders and all are connected to the output of one or more power supply chassis. The resistors are included in the dc power distribution drawing.

The selenium rectifiers are used in power control circuits. Table A-3 of the appendix lists the circuits and drawings in which the sixteen rectifiers are used.

Two of the three potentiometers on this panel are used in the low clock alarm circuit. Resistors R10 (Figure 1-5, 16) and R11 (Figure 1-5, 15) are initial setup adjustments for calibrating the voltage monitor-to-clock signals. Resistor R12 (Figure 1-5, 17) regulates the amplitude of the clock output signals.

The meter relay (Relay 31) is used to detect for abnormal head-to-drum spacing and the three pyrometers, (R20, R21, R22) are used to detect the over-

heating of any of the drum components.

The three mounting boards, MB1, MB2, and MB12, (Figure 1-5, items 14, 12, 13 respectively) are used to mount the remaining components required for the circuitry of this panel (See section 2.7., Mounting Boards and Addressing System). The wiring of this panel is shown in the Bleeder Resistor Panel drawing, DX808,080.

1.2.6 Relay Panel

The relay panel (Figure 1-6) contains 21 relays and two connector plugs (CP54 and CP55, items number 22 and 23 in Figure 1-6). The wiring of this panel is shown in the Relay Box drawing. The name and number of each relay is listed in Table A-1 in the appendix.

1.2.7 Power Control Tray

The power control tray (Figure 1-7) contains three transformers, six relays, a barrier strip, and two mounting boards (See section 2.7).

Transformers T2 and T3 (Figure 1-7, items 5 and 6 respectively) are part of the drum alternator circuit and transformer T4 (Figure 1-7, 12) is the clock filament transformer.

The six relays and the one barrier strip are listed by number, name, and location in the appendix.

The mounting boards, MB13, and MB14 (Figure 1-7, 2 and 3) are used to mount miscellaneous circuitry components.

1.2.8 Power Connectors

Three connectors, shown in figure 1-2a, are used to supply power to the input-output devices. Each connector is colored to match the connector mounted in the particular device it supplies. Green connector socket CS53 (Figure 1-2a) supplies the Card Reader. Yellow connector CS51 (Figure 1-2a) supplies power to the High Speed Printer. Blue connector CS51 (Figure 1-2a) supplies the Read Punch. The wiring of each connector is shown in the Connector Wiring drawings supplied with the computer.

1.2.9 Alternator and Drive Motor

The alternator drive motor (Figure 1-2a) drives the alternator to supply power to the drum motor. The alternator is located directly behind the drive motor.

1.2.10 Blower System

The main blower (Figure 1-2a), driven by the blower motor (Figure 1-3a), circulates air around the packages. Two smaller blower units are used to circulate air about the storage drum and a fourth small unit circulates air through the clock chassis.

1.3 PACKAGE AREA

The fixed bay (Figure 1-8, 1) of the package area contains most of the

FIGURE 1-5 BLEEDER RESISTOR AND RECTIFIER BOARD

1. R3
2. R4
3. R1
4. R9
5. R5
6. R6
7. R2
8. R8
9. R7
10. Selenium Rectifier (SR1 to SR8)
11. Selenium Rectifier (SR9 to SR16)
12. MB2
13. MB12
14. MB1
15. R11
16. R10
17. R12

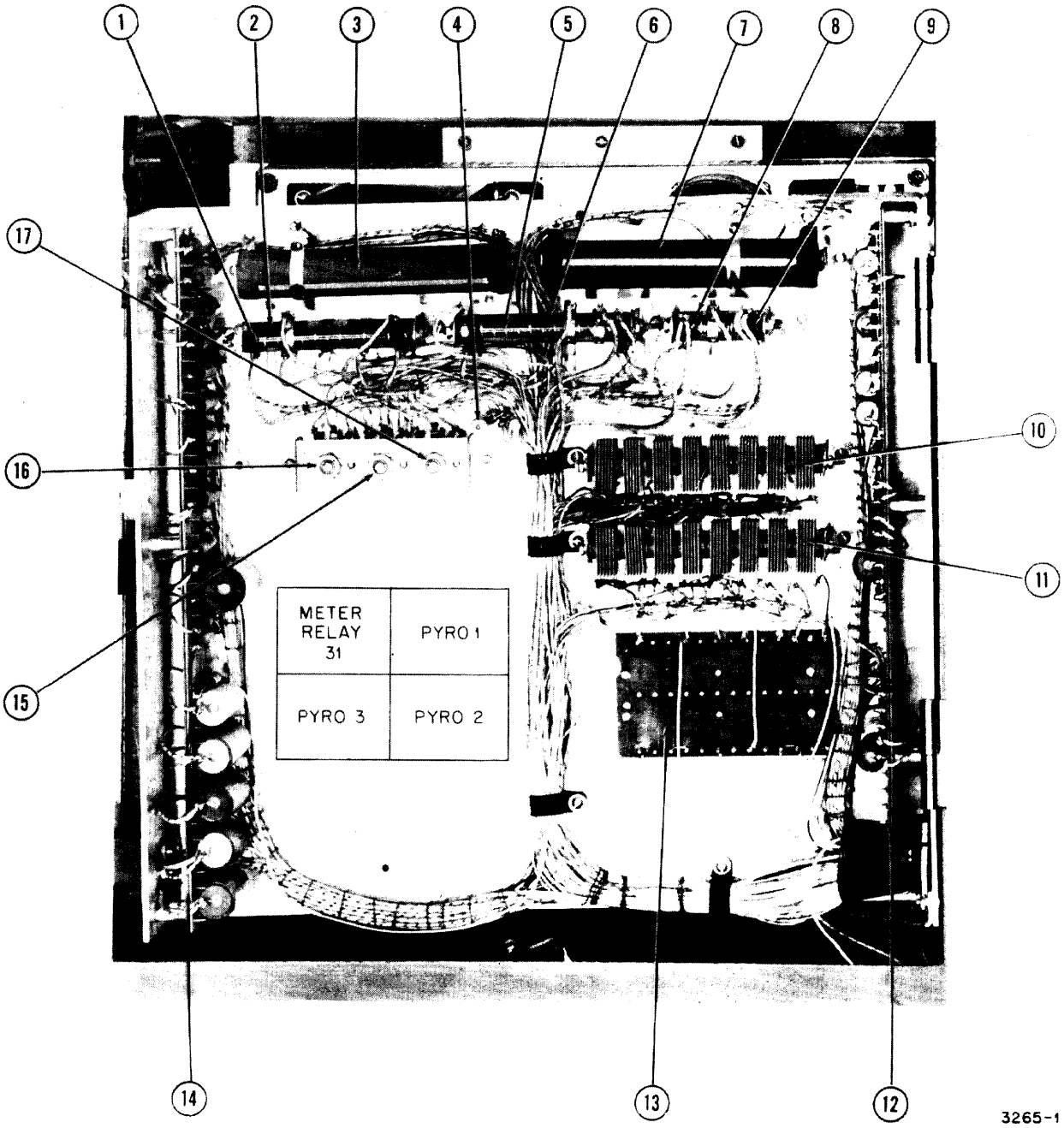


Figure 1-5 Bleeder Resistor and Rectifier Board

FIGURE 1-6 RELAY BOX

1. Relay 23 Fast Reader Off Normal
2. Relay 28 Input Ready
3. Relay 14 DC Fault
4. Relay 13 AC Fault
5. Relay 3 Blower Holdover
6. Relay 30 Memory Write Inhibit
7. Relay 29 P.S. Short Circuit
8. Relay 32 Clock Alarm
9. Relay 33 Drum Alarm
10. Relay 24 Start
11. Relay 19 General Clear
12. Relay 10 DC Ready
13. Relay 8 Drum Ready
14. Relay 18 -DC Alarm
15. Relay 17 +DC Alarm
16. Relay 16 AC Alarm
17. Relay 15 Standby Alarm
18. Relay 5 Air Flow and Air Temp.
19. Relay 20 Processor Off Normal
20. Relay 21 High Speed Printer Off Normal
21. Relay 22 Read Punch Off Normal
22. Connector CP54
23. Connector CP55

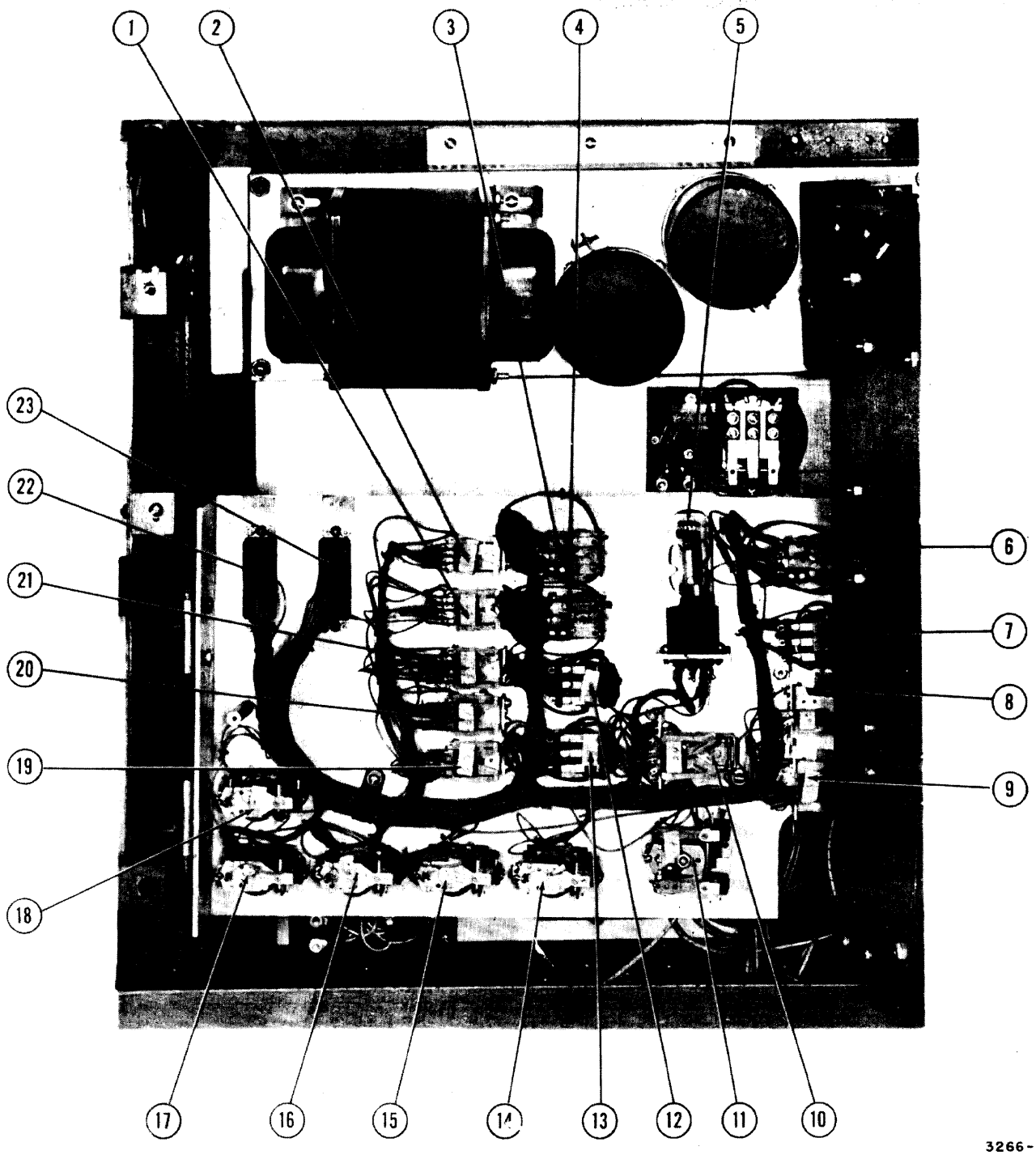


Figure 1-6 Relay Box

FIGURE 1-7 POWER CONTROL TRAY

1. +45V Power Supply
2. MB13
3. MB14
4. Relay 34 Drum Motor Start
5. T2 Drum Alternator Circuit
6. T3 Drum Alternator Circuit
7. Relay 26 Overcurrent +3V
8. Relay 25 Overcurrent +3V
9. Barrier Strip 33
10. Relay 7 Drum Relay
11. Relay 9 DC Delay (2min.)
12. T4 Filament XFMR

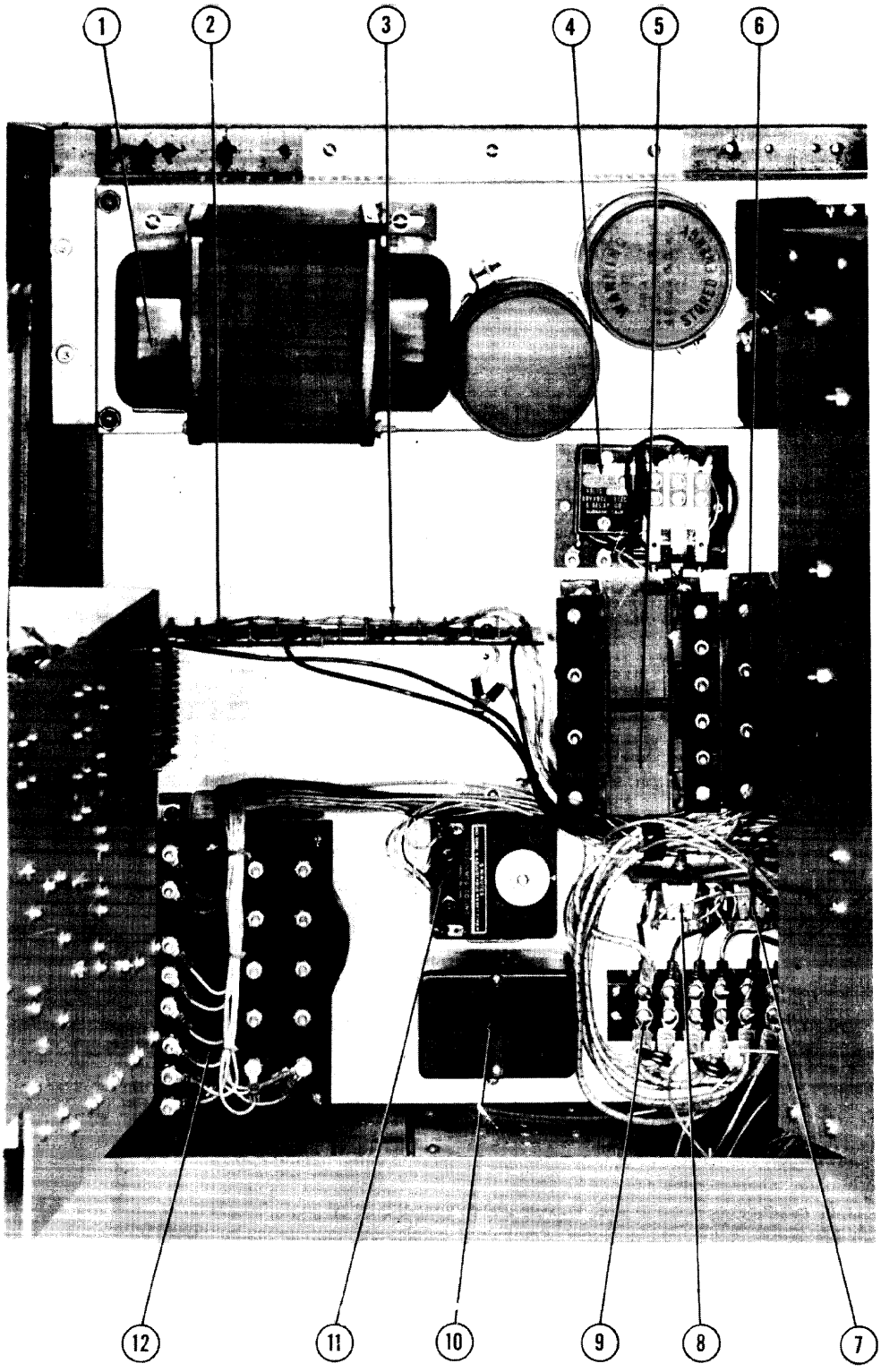


Figure 1-7 Power Control Tray

input-output packages, and the hinged bay (Figure 1-8, 7) contains the packages of the arithmetic unit.

The bays are connected to the frame of the power supply unit and positioned back to back so that packages can be replaced without moving the hinged bay. The hinged bay can be swung out to expose the backboard wiring when it becomes necessary to check the package connections.

Each bay consists of eleven shelves of packages. The shelves of the fixed bay are lettered A B C D E F G H J K L from top to bottom and the shelves of the hinged bay are lettered M N P R S T V W X Y Z.

The bays contain busbars, barrier strips, and connectors to distribute power and information signals to and from the packages. Each item contained in the bays is explained in the following paragraphs.

1.3.1 Package and Connector

Each bay has eleven shelves of packages with each shelf capable of holding 100 packages. The packages are numbered 00 to 99 from left to right and are grouped according to functional units. All packages that are used by Register C are grouped together, all those used by the comparator are grouped together, etc. Figures 1-9 and 1-10 show both bays with the logical grouping and package types indicated. Table 1-1 shows all the package types, their key positions, and the quantity of each type used in the UCT.

A normal package requires at least one shelf space. However, a few occupy two or more spaces because of the size of the components. These double types are marked by asterisks in Table 1-1 and by arrows across two spaces in Figures 1-9 and 1-10. The arrowhead indicates the space where the package connector is located.

Packages consist of wiring printed on a plastic board onto which circuitry components are mounted. Indentical wiring patterns are printed on both sides of the board and the component leads are inserted through drilled holes and dip soldered. The wiring patterns are identical on both sides to insure reliability of the circuits and connections. In some cases printed wiring is supplemented by wire jumpers.

Each package has 22 possible input-output terminals (44 bifurcated terminals) along one edge and 10 test terminals along the opposite edge. The input-output terminals (Figure 1-11) located on the end of the package that fits into the package connector, are numbered 1 to 22 on the component side and 31 to 52 on the solder side. Since the wiring on both sides is identical and common, the terminals by pairs are also common. That is, 1 and 31, 2 and 32, are electrically the same point. Not all of the input-output and test terminals are used.

The package plugs into a connector that is mounted on the shelf to provide

connections for the inputs and outputs of the package. The package connector (Figure 1-8, 6) is equipped with tabs on one side and sockets on the opposite side. On the side into which the package is inserted the socket is a slot with 22 pairs of spring-tension contact points which exert pressure to hold the package firmly. On the wiring side are 22 pairs of tabs onto which the backboard wiring is connected.

The tabs of the connector are numbered the same as the terminals of the package. Each tab of a pair is common to the other tab of the same pair. The use of bifurcated contacts permits the connection of two leads to the same printed circuit when necessary.

Wires are fitted with tab receptacles that fit firmly onto the tabs. A slight leverage is required to connect or remove the tab receptacle from the tab. A special tool is used to grip the tab receptacle when connecting it to a tab.

Keying In Figure 1-11, terminal position 9, 39 has a slot in place of the terminals. This indicates the key position of the package. The connector designed for this type package will have a ridge in position 9, 39 to fit the slot of the package. On the wiring side of the connector, tab position 9, 39 has no tabs. Each package has a key position to prevent one type of package being inserted in a connector designed for another type package. Two or more different types of packages may be keyed at the same position because there are 46 types of packages and only 20 key positions. The top and bottom terminals positions are not used as key positions. However, the packages are laid out in the bays so that package types with the same key are not next to each other.

Test Terminals The test terminals (Figure 1-11) are located on the end opposite the input-output terminals to enable signals to be tested without swinging the hinged bay open. The test terminals are numbered 1 to 10 from top to bottom. Wire jumpers connect them to the component positions. One package, type CSP, uses 15 test terminals instead of the ordinary ten. The extra five, numbered 11 to 15, are located in another vertical row beside the first ten test terminals.

Addressing of Components The components of a package are named on the package circuitry drawing according to their address on the board. As illustrated in Figure 1-11 there are five rows of mounting positions labeled J, K, H, M, and N. The address consists of the initial letter of the component (D for diode, etc.), a letter designates a row and a number of the specific mounting position in the row. Thus, a diode mounted on position 3 of row J would be called DJ3 (Figure 1-11). The bottom mounting position for a component is not given. The length of the component determines to what row the bottom connection would be made. The one notation DJ3 is sufficient to locate the component on the board.

A board which contains magnetic cores has four circular (Figure 1-11,

FIGURE 1-8 PROCESSOR PACKAGE BAYS, BACKBOARD VIEW

1. Fixed Bay
2. Shelf Edge Connector
3. Clock Driver Chassis
4. Signal Cable Between Bays
5. Shelf Edge Connector
6. Package Connector
7. Hinged Bay
8. Bypass Capacitor (+3V to G) (1.5ufd 200V 10%)
9. **MB9**
10. Connector CP72, Signals to and from the Engineer's and Operator's Panel
11. Connector CP71, Signals to and from the Engineer's and Operator's Panel
12. Connector CP70, Signals to and from the Engineer's and Operator's Panel
13. Barrier Strips (BS16, BS35, BS39)
14. Barrier Strips (BS12, BS36, BS38)
15. Connector (CS73 and CP73), Signals to and from the Engineer's and Operator's Panel
16. Connector CPB (Dark Blue), Signals to and from Read Punch Unit
17. Connector CPC (Yellow), Signals to and from High Speed Printer
18. Connector CPD (Green), Signals to and from Card Reader
19. Connector CPA (Light Blue), Signals to and from Read Punch Unit
20. **MB11**
21. Busbar Assembly

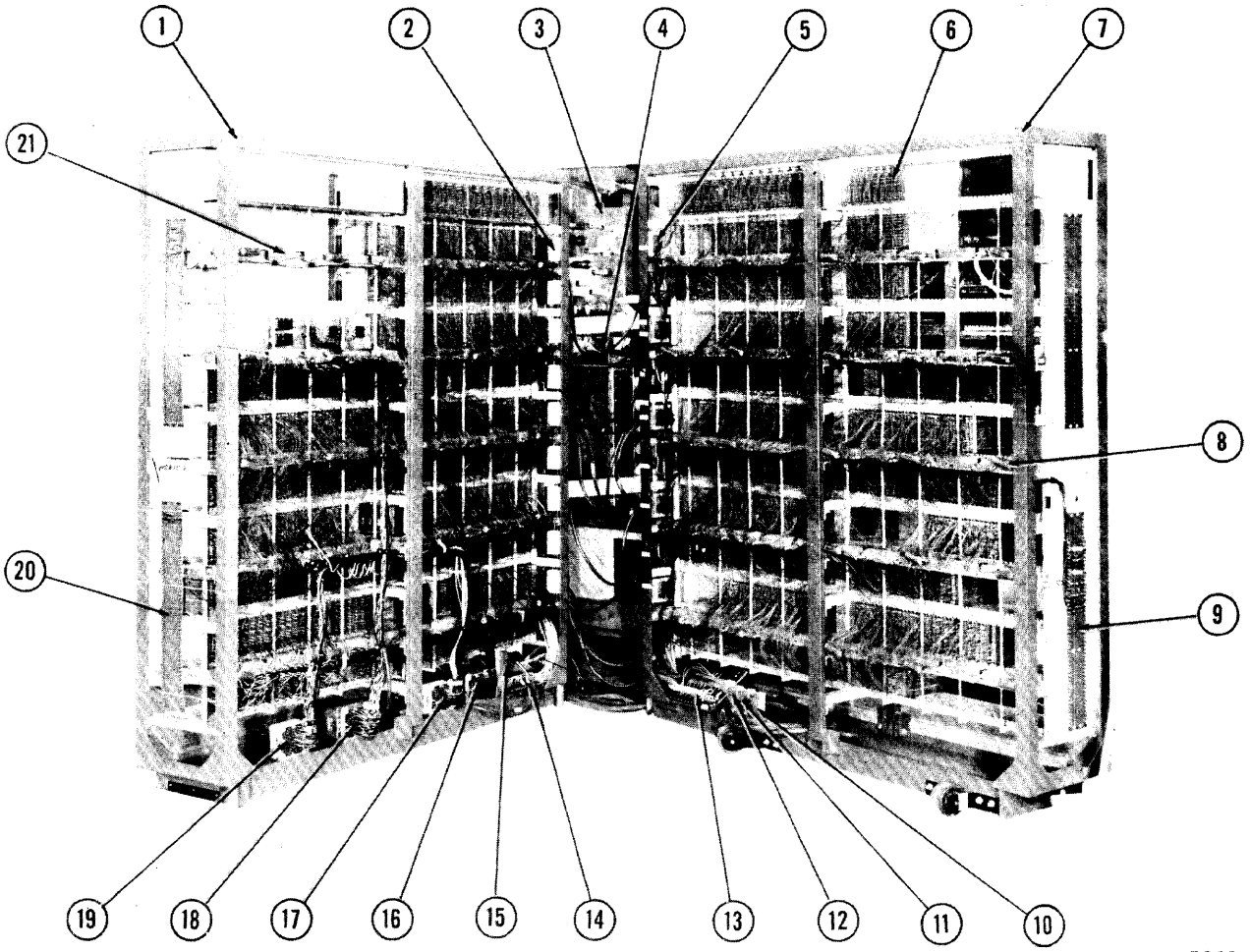


Figure 1-8 Processor Package Bays, Backboard View

dotted lines) position patterns replacing row H. These four positions are numbered 1 to 4 on the component side of the board. Individual points in a circular pattern are numbered 1 to 9 in a counterclockwise direction. Components mounted in these positions are, with rare exceptions, usually magnetic cores, which are named Ferractor #1, Ferractor #2, etc.

1.3.2 Power Wiring

1.3.2.1 D.C.

All dc voltages are distributed within the package area from barrier strips. Seven barrier strips on the end of the fixed bay (Figure 1-8, 1) and three in the base of each bay (Figure 1-8, 13 and 14) receive dc voltages from the power supply chassis. The three in the base also carry control power to the thermostats and card bay interlocks. The leads from the barrier strips in the fixed bay are connected directly to the packages in the fixed bay and to packages in the hinged bay by means of shelf-edge connectors with the exception of the +3V and -29V distribution, explained below. The same is true in the distribution of voltages from the barrier strips in the hinged bay. Shelf-edge connectors are explained in section 1.3.2.4.

NOTE:

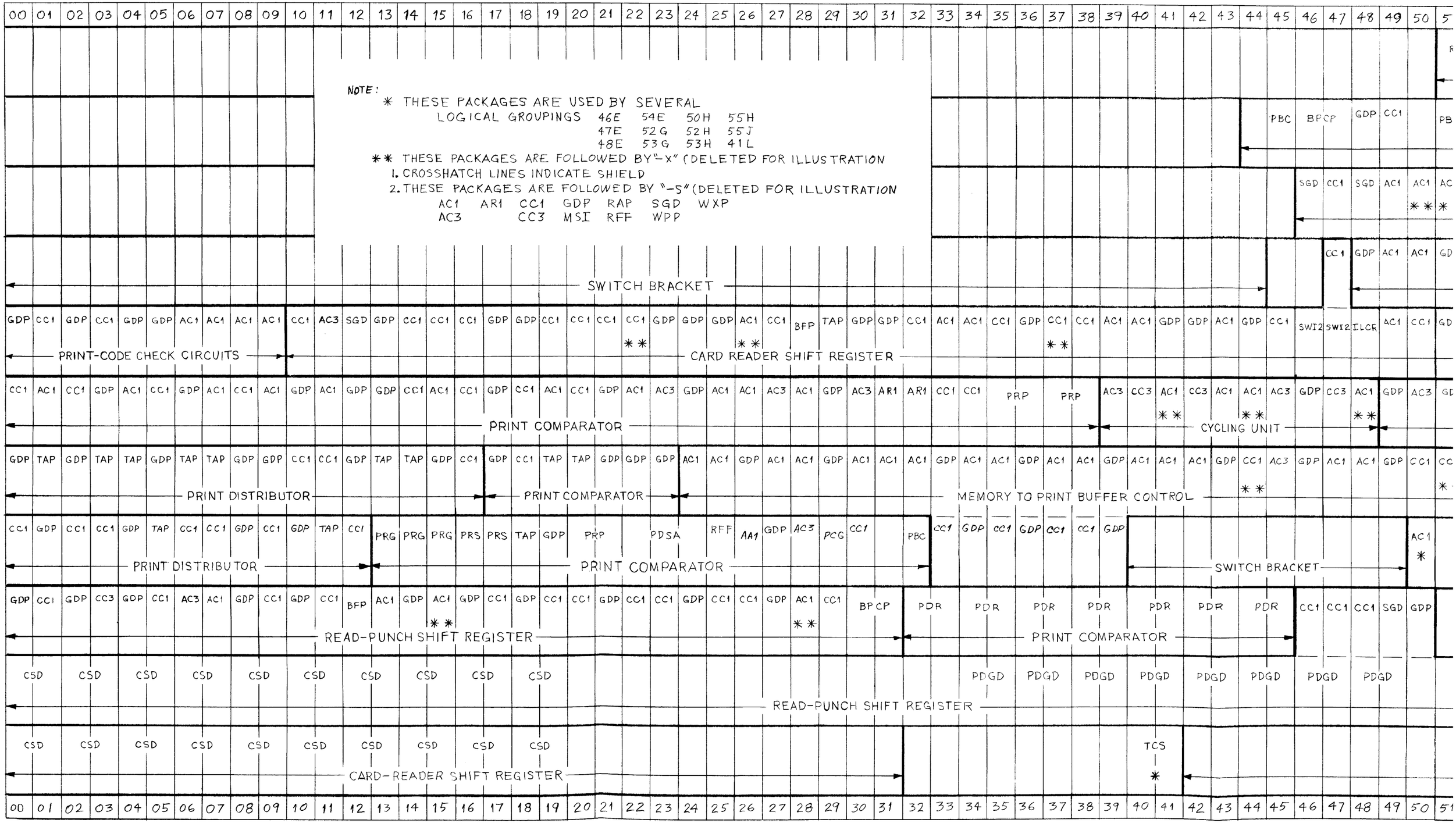
* THESE PACKAGES ARE USED BY SEVERAL LOGICAL GROUPINGS

46E	54E	50H	55H
47E	52G	52H	55J
48E	53G	53H	41L

** THESE PACKAGES ARE FOLLOWED BY "-X" (DELETED FOR ILLUSTRATION

1. CROSSHATCH LINES INDICATE SHIELD
2. THESE PACKAGES ARE FOLLOWED BY "-5" (DELETED FOR ILLUSTRATION

AC1	AR1	CC1	GDP	RAP	SGD	WXP
AC3		CC3	MSI	RFF	WPP	



USED BY SEVERAL
GS 46E 54E 50H 55H
47E 52G 52H 55J
48E 53G 53H 41L
OLLOWED BY "-X" (DELETED FOR ILLUSTRATION
ATE SHIELD
OLLOWED BY "-S" (DELETED FOR ILLUSTRATION
GDP RAP SGD WXP
MSI RFF WPP

SWITCH BRACKET

CARD READER SHIFT REGISTER

CARD BUFFER BANDS 1 AND 2

CYCLING UNIT

MEMORY TO PRINT BUFFER CONTROL

PRINT COMPARATOR

READ-PUNCH SHIFT REGISTER

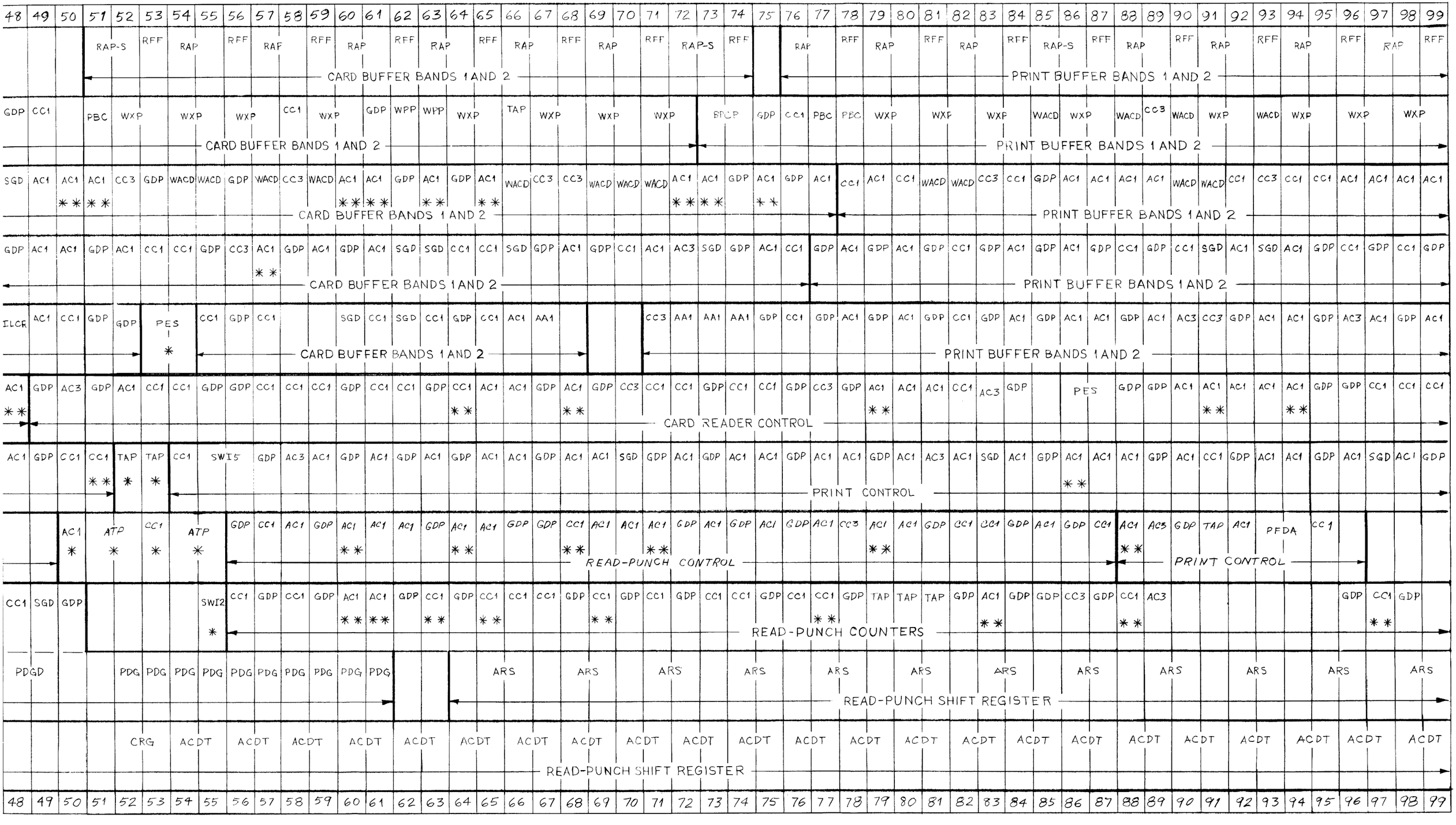


Figure 1-9 Fixed Bay Layout, Shelves A-L

3156

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	5
M	RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF		RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF						
	TIMING-BAND READ CIRCUITS																FAST-NORMAL READ-WRITE CIRCUITS																																							
N	—	PBC		BPCP	*			PBC						PBC			WXP		WXP		CC1	WXP		GDP		WXP		AC1	WXP			WXP		CC1	WXP			GDP	WXP		WXP			WXP		WPP	MSI	MSI	MSI	MSI	MSI	MS
																	FAST-NORMAL READ-WRITE CIRCUITS																																							
P	AC1	AC1	GDP	AC1	AC3	CC3	AC3	AC1	GDP	CC1	AC1	AC1	AC3	CC3	GDP	GDP	CC1	WACD	WACD	CC3	CC1	CC1	GDP	WACD	CC3	CC1	WACD	CC1	CC1	CC1	WACD	AA1	CC1	WACD	WACD	CC3	CC1	GDP	CC1	WACD	CC1	WACD	CC3	CC1	WACD		GDP	CC1	GDP	CC1	GDP	CC
	TIMING-BAND READ CIRCUITS																FAST-NORMAL READ-WRITE CIRCUITS																																							
R														AC1		ILCR	AC1	GDP	GDP	CC1	GDP	AC1	GDP	AC1	SGD	AC1	GDP	GDP	GDP	AC3	AC1	GDP	AC3	AC1	AC1	GDP	GDP	TAP	GDP	CC3	GDP	CC3	GDP	CC1	AC1	GDP	AC3	CC1	GDP	CC1	GDP	AC
																*	FAST-NORMAL READ-WRITE CIRCUITS																																						MEMO
S	GDP	CC1	GDP	CC1	GDP	CC1	GDP	CC1	AC1	GDP	CC1	GDP	CC1	SGD	SGD	GDP	AC1	CC3	GDP	GDP	CC1	SGD	SGD	CC3	SGD	CC3	SGD	SGD	SGD	SGD	SGD	SGD	AC1	SGD	CC3	AC1	GDP	CC1	GDP	GDP	AC1	AC1	GDP	SGD	AC1	AC1	AA1					
																	* *																* *													* *						
	COMPARATOR																																																					
T									AC1	AC1	CC1	GDP	CC1	GDP	AC1	GDP	CC1	AC1	GDP	AC3	GDP	AC1	GDP	SGD	GDP	AC1	CC3	AC1	AC1	GDP	AC1	GDP	CC3	CC3	AC3	GDP	CC3	CC3	AC3	GDP	CC3			AR1	AC1	SGD	AR1	GDP	AR1	AC1	CC1	AC
									SIGN AND CONTROL FLIP-FLOPS																												S BUFFERS																		
V	CC3	AC1	GDP	CC1	CC1	CC3	CC1	CC1	AC1	SGD	AC1	GDP	AC1	AC1	GDP	AC1	SGD	GDP	CC3	GDP	SGD	CC1	CC3	CC1	GDP	AC1	AC1	GDP																		AC1	AC1	GDP	AC1	AC1	GDP	AC1	AR1	AR
							**	**	**		**		**																																								
	FUNCTION ENCODER																																																				
W								SWI5	SWI2	SWI2		CC1	GDP	CC1	GDP	GDP	CC1	GDP	CC3	GDP	CC1	GDP	CC3	GDP	CC1	GDP	GDP	CC1	GDP	CC1	GDP	GDP	CC1	GDP	GDP	CC1	GDP	CC1	GDP	GDP	AC1	GDP	CC3	GDP	GDP	CC3						
								*	*	*		INSTRUCTION DECODER																																												
X	GDP	SGD	GDP	CC1	CC1	GDP	CC1	AC1	CC1	GDP	CC3	CC1	GDP	AC1	CC1	GDP	AC3	CC1	SGD	AC1	CC1	AC1	AC1	CC3	CC3	CC3	AC1	GDP	AC3	AC3	AC1	AC1	GDP	AC1	AC1	CC3		ILCR	GDP	CC1	GDP	CC3	AC3	GDP	SGD	CC1	CC1	CC1	GDP	CC1	GDP	AC
																							**				**							**				*													
	INTERUPTED OPERATION																CYCLING UNIT																																						
Y														CC3	CC1	GDP	TAP	SPS	GDP	CC1	GDP	CC3	AC1	GDP	AC1	GDP	AC1	GDP	AC1	GDP	CC1	GDP	AC1	GDP	CC3	GDP	AC1	GDP	CC3	GDP	AC1	AC1	AC1	AC1	AC1	AC1					GDP	AC
																								**			**						**																			
	MULTIPLIER QUOTIENT COUNTER																																																		
Z	RDP	RDP	RDP	RDP	RDP	RDP	RDP	RDP	RDP	RDP	RDD																					AC1	GDP	AC1	AR1	AR1	AR1		AA1	GDP	AC1	GDP	AC1	AR1	AR1	AR1		AA1	AC1	GDP	AC1	AI
	REGISTER C																															REGISTER L																					
	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	5

23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75
P	RFF	RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF	RAP		RFF					MSP	MSP	MSP	MSP	MSP	MSP	MSP																				
FAST-NORMAL READ-WRITE CIRCUITS																												MEMORY SELECTION																										
GDP		WXP		AC1	WXP			WXP		CC1	WXP			GDP		WXP		WXP			WXP	WPP	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI	MSI											
RMAL READ-WRITE CIRCUITS																												MEMORY SELECTION																										
WACD	CC3	CC1	WACD	CC1	CC1	CC1	WACD	AA1	CC1	WACD	WACD	CC3	CC1	GDP	CC1	WACD	CC1	WACD	CC3	CC1	WACD		GDP	CC1	GDP	CC1	GDP	CC1	GDP	CC1	GDP	CC1	GDP	CC1	CC1	GDP	CC1	GDP	CC1	GDP	CC1	GDP											
FAST-NORMAL READ-WRITE CIRCUITS																							MEMORY SELECTION																										
AC1	SGD	AC1	GDP	GDP	GDP	AC3	AC1	GDP	AC3	AC1	AC1	GDP	GDP	TAP	GDP	CC3	GDP	CC3	GDP	CC1	AC1	GDP	AC3	CC1	GDP	CC1	GDP	AC1	SGD	GDP	AC1	CC1	CC1	GDP	CC1	CC1	GDP	CC1	GDP	AC1	CC1	AC1										
FAST-NORMAL READ-WRITE CIRCUITS																							MEMORY SELECTION																										
CC3	SGD	CC3	SGD	SGD	SGD	SGD	SGD	SGD	AC1	SGD	CC3	AC1	GDP	CC1	GDP	GDP	AC1	AC1	GDP	SGD	AC1	AC1	AA1													GDP	GDP	CC1	GDP	GDP	CC1	CC1	CC1	SGD	SGD	CC3	AC3	GDP	GDP	CC1	CC1
ARATOR																																																				
SGD	GDP	AC1	CC3	AC1	AC1	GDP	AC1	GDP	CC3	CC3	AC3	GDP	CC3	CC3	AC3	GDP	CC3			AR1	AC1	SGD	AR1	GDP	AR1	AC1	CC1	AC1	AR1	AC1	AC1	GDP	AC1	AC1	GDP	AC1	CC1	AC1	AC1	AC1	GDP	AR1	AC1	AC1	GDP	AR1	AC1	GDP	AC1	AC1	AC1	GD
-FLOPS										S BUFFERS										REGISTER X																																			
CC1	GDP	AC1	AC1	GDP																AC1	AC1	GDP	AC1	AC1	GDP	AC1	AR1	AR1	AR1	GDP	SGD	AC1	AC1	GDP	AC1	AR1	AR1	AR1	GDP	AC1	AC1	GDP	AC1	CC1	SGD	AR1	AR1	AR1	GDP	AC1	GDP	GDI
REGISTER A																																																			
CC3	GDP	CC1	GDP	GDP	CC1	GDP	CC1	GDP	GDP	CC1	GDP	GDP	CC1	GDP	GDP	AC1	GDP	CC3	GDP	GDP	CC3																								AC1	AC1	GDP	AC1	GDI
INSTRUCTION DECODER																																																		
CC3	CC3	CC3	AC1	GDP	AC3	AC3	AC1	AC1	GDP	AC1	AC1	CC3		ILCR	GDP	CC1	GDP	CC3	AC3	GDP	SGD	CC1	CC1	CC1	GDP	CC1	GDP	AC1	GDP	CC1	GDP	CC1	GDP	AC3	GDP	CC3	CC1	AC3	CC3	AC3	CC3	GDP	CC1	CC1	GDP	AC3	CC3	CC3	CC1	GDP	AC1	AC1
CYCLING UNIT																STATIC REGISTER																																						
GDP	AC1	GDP	AC1	GDP	AC1	GDP	CC1	GDP	AC1	GDP	CC3	GDP	AC1	GDP	CC3	GDP	AC1	AC1	AC1	AC1	AC1	AC1					GDP	AC1	AR1	AC1	AR1	AA1	AR1	GDP	AC1	AA1	AC1	AR1	AC1	GDP	AA1	AR1	AR1	AC1	GDP	AA1	AC1	AR1		AR1	GDP	
MULTIPLIER QUOTIENT COUNTER																																																			
								AC1	GDP	AC1	AR1	AR1	AR1		AA1	GDP	AC1	GDP	AC1	AR1	AR1	AR1		AA1	AC1	GDP	AC1	AR1	AR1	AR1			GDP	AC1	GDP	AC1	AR1	AR1	AR1	AA1													
REGISTER L																																																			
23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75

NOTE:
*
**
1.
2.

MEMORY SELECTION

MEMORY SELECTION

MEMORY SELECTION

M BUFFERS

REGISTER X

REGISTER A

QUINARY ADDER

STATIC REGISTER

REGISTER C

REGISTER L

NOTE:

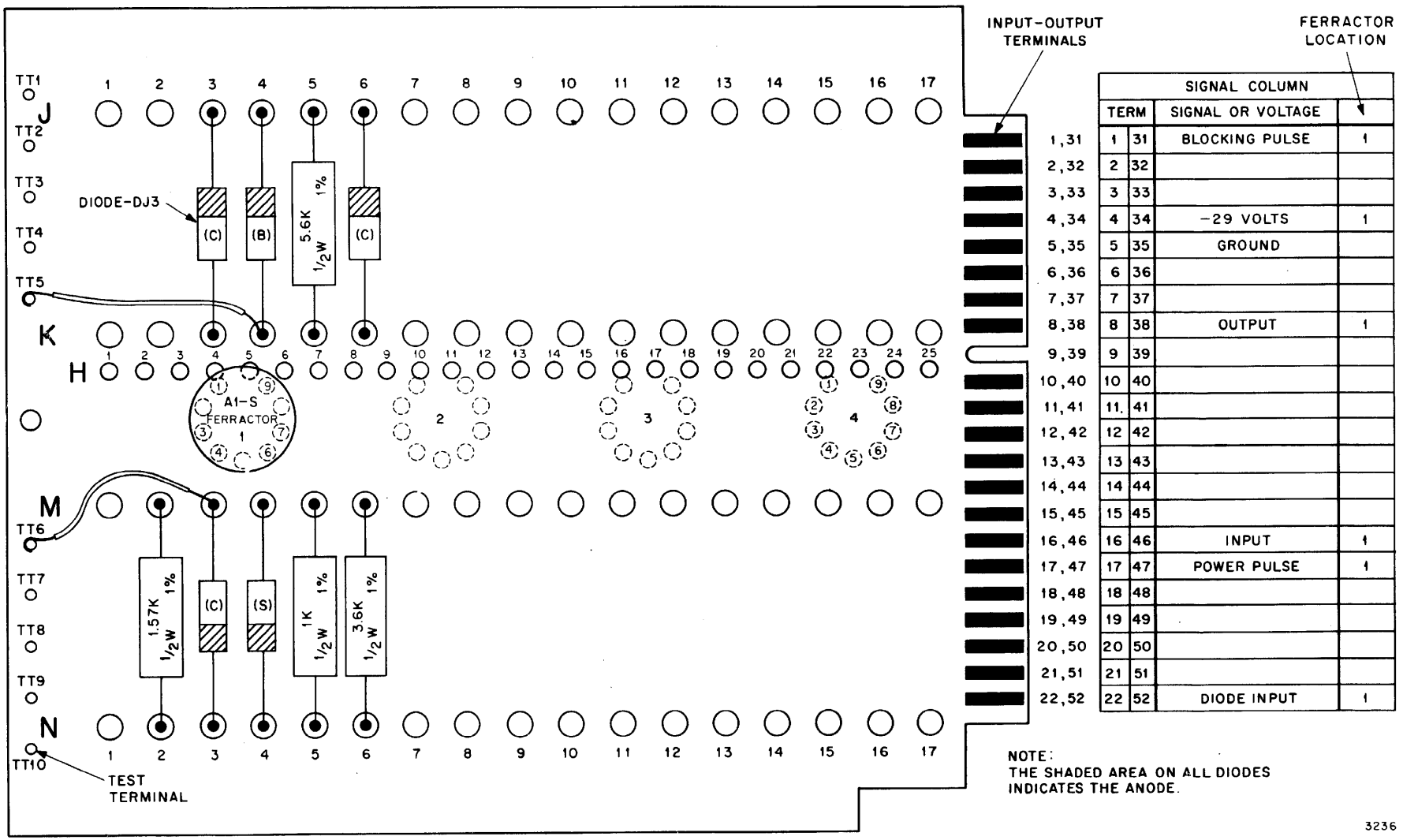
* THESE PACKAGES ARE USED BY SEVERAL LOGICAL GROUPINGS 04N 15R 8W 9W 10W 37X 76X

** THESE PACKAGES ARE FOLLOWED BY "-X" (DELETED FOR ILLUSTRATION)

1. CROSSHATCH LINES INDICATE SHIELD
2. THESE PACKAGES ARE FOLLOWED BY "-S" (DELETED FOR ILLUSTRATION)

AC1 AR1 CC1 GDP RAP SGD WXP
AC3 CC3 MSI REF WPP

Figure 1-10 Hinged Bay Layout, Shelves M-Z



	SIGNAL COLUMN			
	TERM		SIGNAL OR VOLTAGE	
1,31	1	31	BLOCKING PULSE	1
2,32	2	32		
3,33	3	33		
4,34	4	34	−29 VOLTS	1
5,35	5	35	GROUND	
6,36	6	36		
7,37	7	37		
8,38	8	38	OUTPUT	1
9,39	9	39		
10,40	10	40		
11,41	11	41		
12,42	12	42		
13,43	13	43		
14,44	14	44		
15,45	15	45		
16,46	16	46	INPUT	1
17,47	17	47	POWER PULSE	1
18,48	18	48		
19,49	19	49		
20,50	20	50		
21,51	21	51		
22,52	22	52	DIODE INPUT	1

Figure 1-11 Package Pictorial

TABLE 1-1. Packages Used in the UCT

Package Designation	Type of Package	Key Position	Quantity
AA1	Single power amplifier	7,37	21
AC1-S	Single power amplifier, complementer	9,39	274
AC1-X	Special single power amplifier, Complementer	21,51	
AC3-S	Double power amplifier, complementer	12,42	35
ACDT-II*	Actuator column driver	5,35	23
AR1-S	Arithmetic register	3,33	47
ARS*	Tower punch actuator row switch	6,36	12
ATP*	Actuator transistor	13,43	2
BFP	Bit filter	13,43	2
BPCP*	By-Pass capacitor	14,44	
CC1-S	Single power complementer	11,41	223
CC1-X	Special Single power complementer	2,32	
CC3-S	Double power complementer	8,38	62
CGDT*	Clear generator driver tower	14,44	1
CGT*	Clear generator tower	13,43	1
CRG*	Column reset generator	13,43	1
CSD*	Capacitor sense driver	21,51	32
CSGP	Capacitor storage gating	13,43	4
CSP-II	Capacitor storage	14,44	50
GDP-S	Gating diode	10,40	322
ILCR*	Indicator light, choke	13,43	4
MSI-S-II	Head switch driver	4,34	20
MSP-II*	Matrix selector position	2,32	7
PBC	Probe Clear	13,43	8
PCG	PC generator	13,43	1
PDG	Punch Information distribution	14,44	10
PDGD-II*	Punch distribution gate driver	20,50	8
PDR-II*	Print drum read amplifier	14,44	7
PDSA**	Print drum sprocket amplifier	13,43	1
PES*	Printer noise suppressor	18,48	
PFDA* III	Paper feed drum amplifier	13,43	1
PRG	Print gate	13,43	3
PRP*	Print sample	19,49	3
PRS	Print set	14,44	2
RAP-S-IV*	Read amplifier	16,46	31
RDD-II	Register display driver	13,43	1
RDP	Register display	14,44	10
RFF-S	Read amplifier flip-flop	17,47	32
SGD-S	Special gating diode	13,43	45
SPS	Sprocket shaper	14,44	1

Package Designation	Type of Package	Key Position	Quantity
SW12	Switch input circuits to mag. amps.	14,44	4
SW15*	Switch input circuits to mag. amps.	13,43	1
TAD	Tower actuator diode	7,37	30
TAP	Transistor amplifier	18,48	18
TCS*	Tower cam synchronizer	13,43	1
TSD	Tower sensing diode	20,50	60
WACD	Write amplifier and complementer drive	20,50	26
WPP-S-II	Write pedestal	13,43	3
WXP-S-II*	Write transformer	15,45	26

* Double Shelf Space Required
** Triple Shelf Space Required

The +3V and -29V are distributed to all magnetic amplifier packages by means of busbars. The barrier strip leads are connected to horizontal busbars between the shelves (Figure 1-12). The package leads are connected to tabs on the busbar. The busbars are explained in section 1.3.2.3.

1.3.2.2 Power and Blocking Pulses

The clock circuit develops A- and B- phase pulses which are sent to every magnetic amplifier package. The clock output transformer is connected directly to the vertical busbars in the power supply section which in turn are connected to the vertical busbars of the hinged and fixed bays (Figure 1-12) and the horizontal busbars between the shelves. The A- and B- phase blocking pulses are supplied to the horizontal busbar from a transformer mounted on the shelves at the end of each busbar assembly. The A- and B-phase power pulses enter the transformer and are stepped down to the blocking pulse level.

1.3.2.3 Busbars

There are five busbar assemblies (Figure 1-8, 21) mounted in each bay between the shelves to supply voltage, power pulse, blocking pulse, and ground connections to the packages.

The top shelf of each bay does not require busbar connections so the first busbar assembly in the fixed bay is between shelves B and C and the first busbar assembly in the hinged bay is between shelves N and P. Each busbar assembly is identified by the shelves it feeds. Thus, B-C would be the top busbar assembly in the fixed bay and N-P the top busbar assembly in the hinged bay. The five busbar assemblies in the fixed bay are: B-C, D-E, F-G, H-J, K-L; and in the hinged bay: N-P, R-S, T-V, W-X, and Y-Z.

Seven busbars are mounted in each busbar assembly with spacers and insulators. The busbars are made of brass coated with iridite, the spacers of brass and the insulators of Teflon and Mylar.

One edge of the horizontal busbars is formed into tabs identical to the tabs on the package connector to which the package wiring is connected. The tabs of the busbars are not numbered or lettered in any way. The connections from the packages are made to the nearest available tab.

The busbars are numbered one thru seven from top to bottom. Busbar 1 carries +3 volt dc, busbar 2 carries the B-phase blocking pulses; busbar 3 carries the A-phase power pulses; busbar 4 is ground; busbar 5 carries the B-phase power pulses; busbar 6 carries the A-phase blocking pulses; and busbar 7 carries -29 volts dc.

The horizontal busbar assemblies mounted between the shelves are connected to vertical busbar assemblies on the end of each bay. The vertical busbar assemblies supply the horizontal busbar with the required voltages and pulses. The vertical busbar assemblies consist of five iridite coated brass busbars clamped together with spacers and insulators.

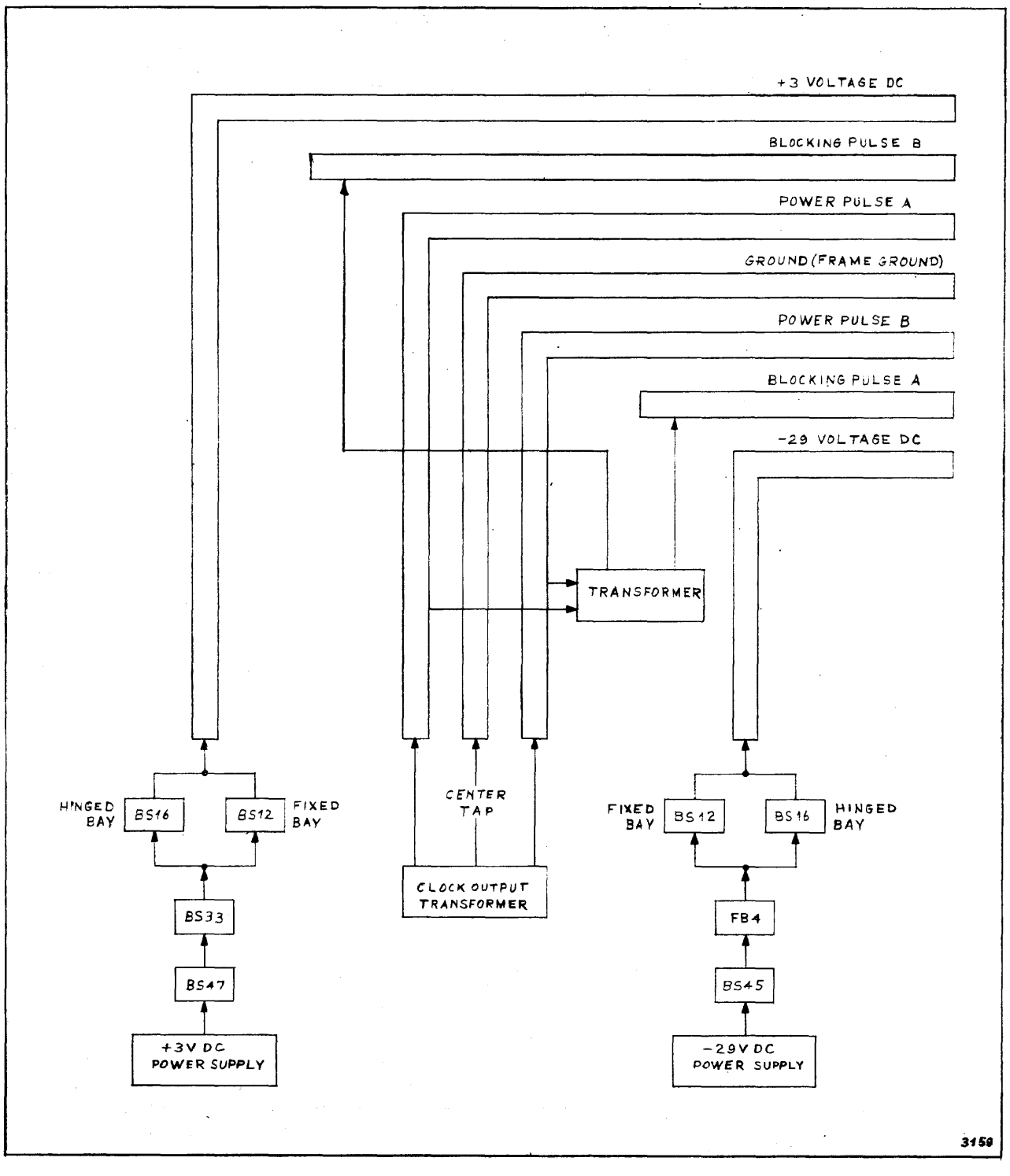


Figure 1-12 Busbar Supply System

The five busbars of the vertical assemblies supply +3 and -29 volts, ground, A and B phase power pulses to the horizontal busbars. The A- and B- phase blocking pulses are supplied from a transformer mounted on the shelves at one end of each busbar assembly. The A- and B-phase power pulses enter the transformer and are stepped down to the blocking pulse level.

The vertical busbars are supplied the A- and B-phase power pulses directly from the clock output transformer. The voltages are supplied from barrier strips in the base of each bay. The ground busbar is grounded to the frame and is also connected to the center tap of the clock output transformer. Figure 1-12 shows the connections of the vertical and horizontal busbar in block diagram form.

1.3.2.4 Shelf-Edge Connectors

The fixed bay contains 9 shelf connectors (Figure 1-8, 2), one on the end of each shelf to serve as a connection point for voltages and signal between bays. Each edge connector has twelve taper pin sockets on both sides. A maximum of five connectors can be inserted on each shelf giving a total of 60 possible sockets. Each connector is identified by the shelf letter and its position in relation to other edge connectors. The five on the B shelf would be edge connectors BA, BB, BC, BD, and BE. BA will be the first one from the wiring side of the bay.

The leads from the packages are connected to one side of the edge connector. On the other side leads are connected into the sockets and carried over to the hinged bay in harness form. The individual leads are connected to a connector socket by means of taper pins. The socket in turn is connected to connector plugs (Figure 1-8, 5) on the end of the equivalent shelf on the **hinged bay.**

The connector plug has taper pin sockets on one side into which leads to and from packages are connected. The socket and plug combination in the hinged bay is used to provide an easy disconnect and eliminates disconnecting the individual leads in the fixed bay.

The connector plug has fifty taper pin sockets on one side and male connectors on the other end. The connector plugs are designated CP60 through CP68 and the connector sockets are designated CS60 through CS68. The lowest number plug is located on the N shelf with the connectors on the other shelves numbered consecutively downward with CP68 on the Y shelf. The connector socket on the end of the harnassed wires fits the connector plug of the corresponding number. Thus, CS60 plugs into CP60, CS61 into CP61, etc. The wiring of each shelf edge connector is shown in the Processor Connector Wiring drawings.

1.3.3 Signal Wiring

Signal wiring consists of leads between packages within one bay, between both bays, between the processor and input-output units, and between packages and the control panels. Signal flow between packages within the same bay is accomplished by connecting a lead between the tabs of the packages involved. Signals between packages in different bays are routed through the shelf-edge connector (Section 1.3.2.4).

Signals between the bays and the control panels are routed through the panel connectors (Figure 1-8, item 10, 11, 12 and 15) in the base of each bay. There are four 50-socket connector plugs mounted in the bays, 3 in the base of the hinged bay and 1 in the base of the fixed bay. These plugs carry signals to and from the control and Engineering Panels. The connectors in the hinged bay are CP70, CP71, and CP72 and the one connector in the fixed bay is CP73. Connector plugs 70, 71, and 73 carry signals to and from the operators panel, CP72 is used mostly for signals to and from the keyboard and Engineering Panel.

The leads to and from packages are connected to the plug by means of taper pins. The plug then fits a connector socket to carry the leads to the panels.

Signals between the package area and the input-out-put units are sent through the four connectors (Figure 1-8, items 16-19) in the base of the fixed bay. Signals from the hinged bay are first routed through the shelf-edge connectors, then to the input-output connectors.

The four connectors are named CPA (light blue), CPD (green), CPC (yellow), and CPB. Each connector is colored to match the connector in the particular input-output unit it supplies.

The signal leads are connected by taper pins to the connector sockets. A connector plug attached to harnassed leads fits the plug to carry the signals. to the necessary equipment. The harnassed leads have a connector socket to fit a plug mounted in the accessory are labeled CPA, etc. The connector sockets mounted in the fixed bay and the sockets on the harnassed wires are labeled CSA, etc. The connector socket CSC in the fixed bay receives connector plug CPC which is on one end of the harnassed wires. The connector plug in the printer is also CPC and it fits into connector socket CSC on the harnassed wires. CSA and CSB carry signals to the Read-Punch Unit, CSC carries signals to the High Speed Printer and CSD carries signals to the Card Reader.

SECTION TWO

PRINTED MAINTENANCE AIDS

2.1 GENERAL

Printed maintenance aids in the file of prints for the computer provide various types of information. The major types of prints are: Logic, Troubleshooting Layout, Wiring, and Schematic.

Logic diagrams, which are discussed in the Processor and Input-Output manuals, describe the logic of UCT circuits. Troubleshooting layouts are expanded versions of logic diagrams showing many physical connection points. Wiring Charts show all terminal-point connections. There are wiring charts for all shelves, connectors, power supplies, fuse panels, barrier strips, etc. Since all wiring charts are of the same type, only the shelf wiring charts are explained in this section.

Pictorial drawings of each package show the circuit components, their positions on the board, and all terminals on the package. (See section 1.3.1, Figure 1-11). Schematic drawings show all of the circuitry of the UCT. There are schematic drawings of packages, power distribution, power controls, controls and indicators, etc. Since most circuits consist of printed wiring, package schematics are explained in this section. Reference drawings such as layout legends, signal lists, processor package complement, and bay layouts are also available as maintenance aids.

Signal lists show all logic signals, together with their source and destination. The complete signal list is contained in Appendix A of the Processor Manual. The processor package complement combined with the bay layouts (see section one, Figure 1-9 and 1-10) show the grouping of the logical units and each package location.

Most diagrams and drawings can be advantageously used in conjunction with others. For example, an input signal can be found at a certain terminal on a particular package on a troubleshooting layout, and then by locating the same terminal and package on the shelf wiring charts, the package type can be found. Next, using a package schematic, the circuit component that the signal enters can be identified, and with a package pictorial it can be located on the package. This section explains the troubleshooting layouts and wiring charts and their use together in tracing signals.

2.2 LOGIC DIAGRAMS

Logic diagrams show only the logical components of UCT circuits and the signal flow between these components. No attempt is made on these diagrams to identify physical locations. The UCT Processor and Input-Output manuals use the logic diagrams to explain the theory of operation of the computer, and Section Two of the Processor manual explains the symbolism used. A complete set of

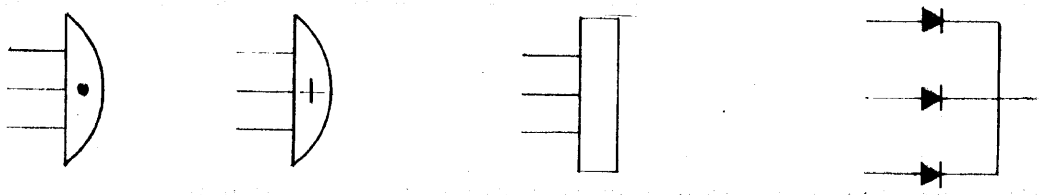
logic diagrams is contained in Appendix A of the Processor manual.

2.3 TROUBLESHOOTING LAYOUTS

Troubleshooting Layouts (also known as Logic Layout Drawings) indicate the package addresses of all logical components and show in detail the physical connections between packages. All troubleshooting layouts use the same symbolism, so the example used in Figure 2-3 will suffice to explain the use of this type.

Figure 2-1 lists all logic symbols and their Troubleshooting Layout counterparts. When an amplifier has a built-in diode, it is indicated by an enclosed corner of the symbol. Figure 2-2a shows a gate feeding an amplifier in both logic and troubleshooting symbolism. In the logical representation of the circuit, four input signals enter a gate symbol, whose output enters an A-phase amplifier. In the troubleshooting representation of the same circuit (Figure 2-2b), three leads enter the gate symbol and the fourth enters the amplifier through the built-in diode.

A gate or buffer consists of a number of diodes with a common output and several inputs. The actual electronic configuration of a buffer or gate is shown below along with its logical and troubleshooting counterparts.



LOGICAL GATE | LOGICAL BUFFER | TROUBLESHOOTING GATE OR BUFFER | ELECTRONIC CONFIGURATION OF GATE OR BUFFER

Sections Two and Six of the Processor manual explain the logical and electronic functions, respectively, of gates and buffers.

The troubleshooting amplifier symbol (Figure 2-2b) has power pulse, blocking pulse, and test terminals indicated. On both logic and troubleshooting symbols (Figure 2-1), a dot on the amplifier symbol indicates that it is a complementer and the letter A or B indicates the phase of the component. The letter S following the phase letter within the symbol indicates an arithmetic-register shift-type core. Similarly, the letter T indicates an arithmetic-register transition-type core. On troubleshooting layouts an output signal is shown within a rectangular box (Figure 2-2) at the vertex of the amplifier symbol. Complete special packages are represented by a rectangle with the package letters inserted for identification.

Figure 2-3 contains parts of four separate packages, all of which are on the Y shelf. The packages involved are numbered 57, 60, 61, and 63. The package-terminal-point is designated by the package number, shelf letter, and

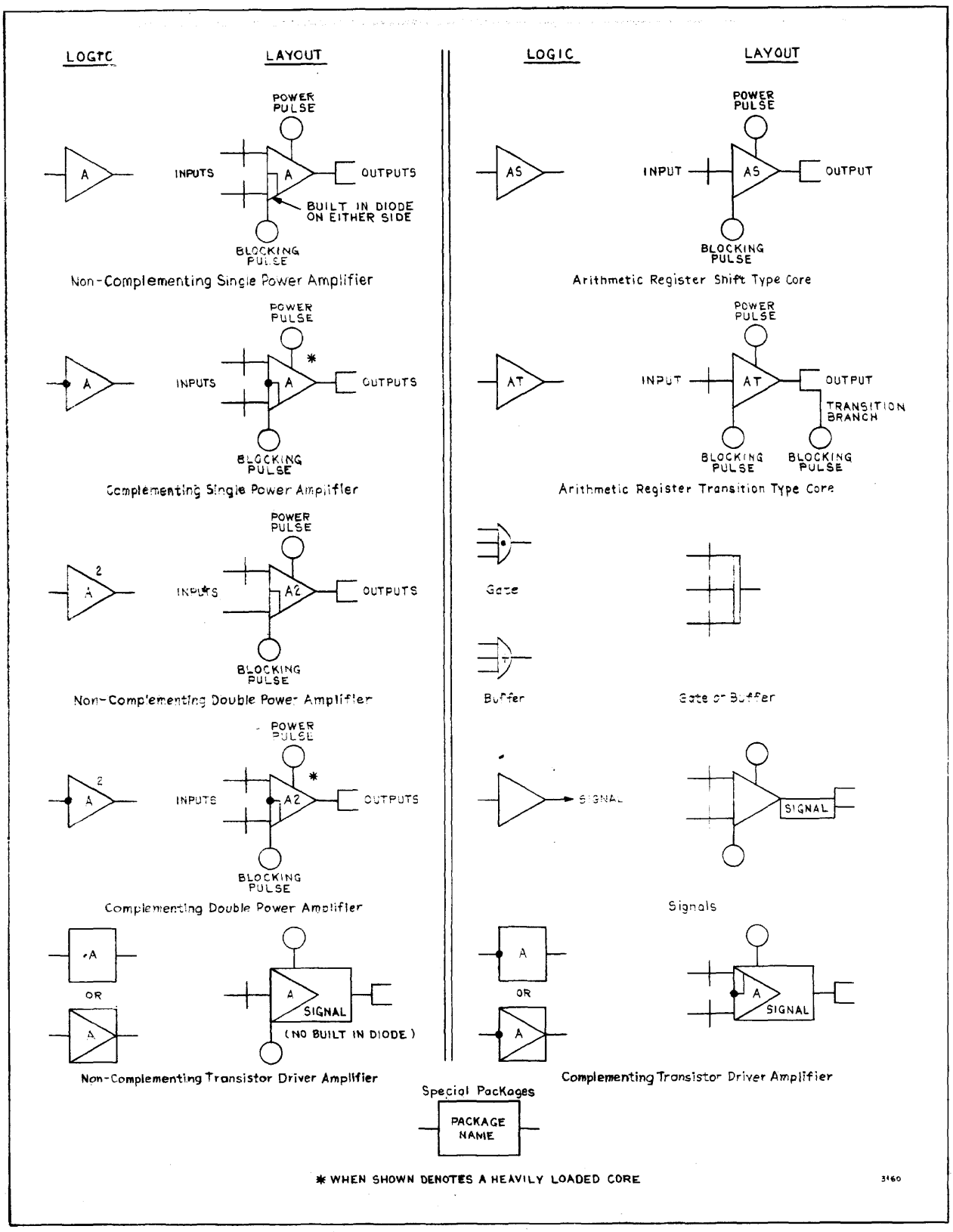


Figure 2-1 Logic and Troubleshooting Symbols

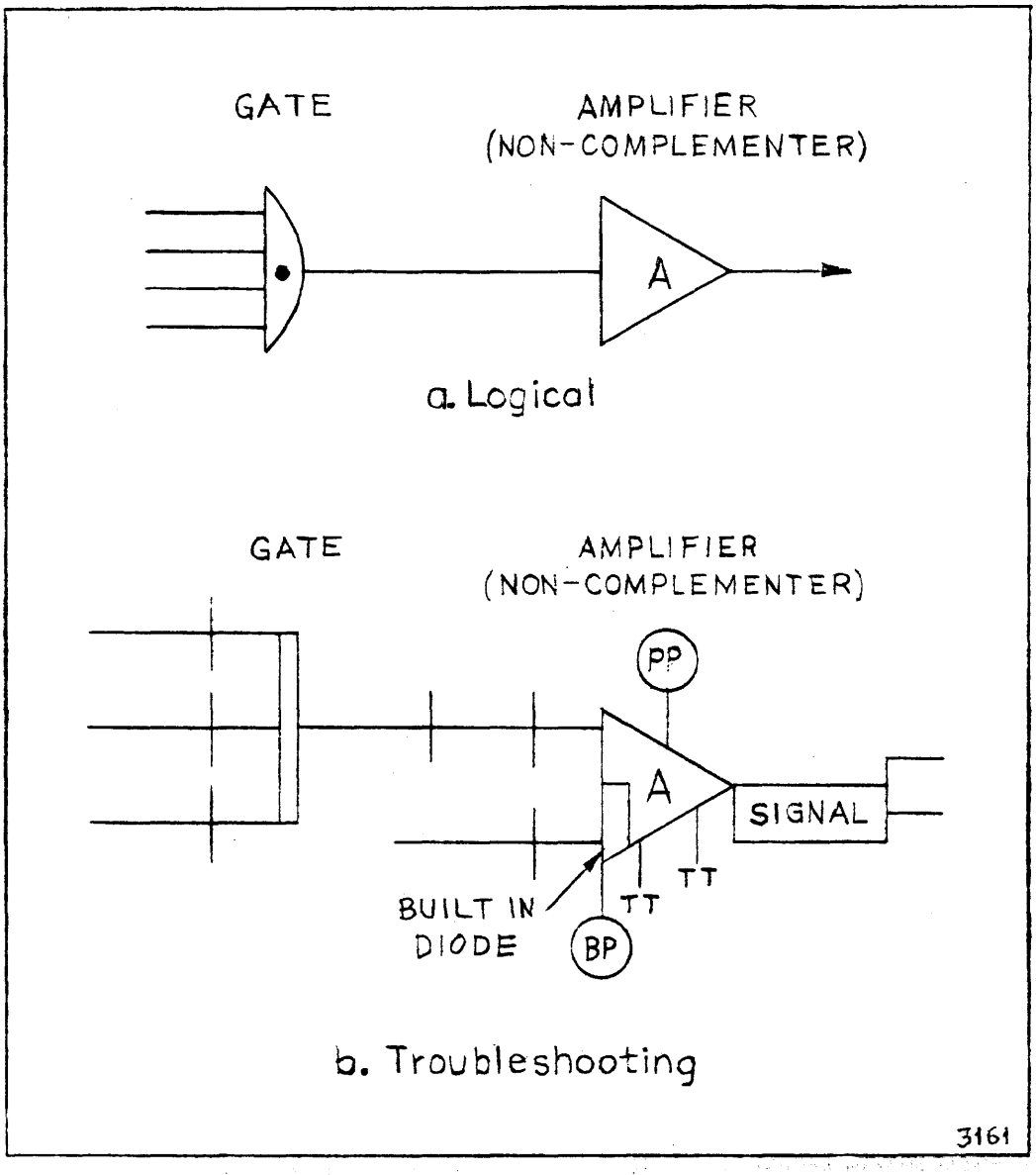
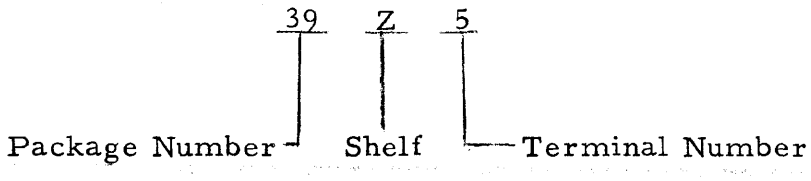


Figure 2-2 Gate and Amplifier Symbols

terminal number. Example:



Three leads are shown connected to the first gate in Figure 2-3 although only one is used. The unused leads are shown for uniformity since many other such components do use all or most of their connections. The broken lines in Figure 2-3 show the separation between packages. Such lines are not found on the actual layouts and are used only to simplify this example.

The first input shown in Figure 2-3 is signal M2 which comes from point 39Z5 and enters package 57Y at terminal point five. It leaves package 57Y at point 35 (57Y35) and also, after flowing through a diode, at point 8 (57Y8). From point 57Y35 it goes to and enters package 52X at point 20 (52X20), and from 57Y8 it enters an A-phase complementer in package 60Y at point eight.

Function signal 2B comes from 51Y52 and enters package 60Y at point 22. Signal 2B leaves package 60 Y at terminal point 52 and enters package 70Y at point 22. It also enters an A-phase complementer in package 60Y through the built-in diode which is indicated by the enclosed corner of the complementer symbol. The complementer is supplied with an A-phase power pulse entering package 57Y at terminal point 17 and with a B-phase blocking pulse entering the package at point six.

The circled numbers 17 and 6 signify only the terminal point at which the power pulse or blocking pulse enters the package and should not be confused with function signals. In all function signals, the number is followed by the letter A or B; for example, function signal 2B enters package 60Y at terminal point 22. The letter A or B signifies the phase of the function signal. Power pulses are always indicated entering a complementer, amplifier, or core from above the symbol, while a blocking pulse enters from below. When the component is A-phase, the power pulse is A-phase and the blocking pulse B-phase, while the reverse is true for B-phase components.

The two lines (TT7 and TT4) shown entering the complementer from below indicate test terminals. The first (TT7) is for testing the input signal while the second (TT4) is for testing output signals. The test terminal for the input is always shown toward the input side of the symbol and the output test terminal is shown on the output end.

The output signal of the complementer in package 60Y goes to point 14 (60Y14), which is one point of a branch in the drawing. The second common terminal point (44) is not used but is included for uniformity. Since point 44 is

not used, it is not labeled on this layout. An example of the use of both bifurcated terminals is the first input on the drawing. Signal M2 from terminal point 39Z25 enters package 57Y at point five and leaves by the corresponding point 57Y35.

The signal leaves package 60Y at point 14 (60Y14) and enters package 57Y at point 22 (57Y22). It flows through a diode in package 57Y to become an output at point 15 (57Y15). From this point the signal leaves package 57Y and enters package 60Y at terminal point 12 (60Y12). The signal goes through a B-phase complementer in package 60Y. An output signal from terminal point 60Y13 also enters the same complementer at point 20 (60Y20), through the built-in diode.

The complementer in 60Y receives a B-phase power pulse through point 19 (60Y19) and an A-phase blocking pulse through point three (60Y3). The signal leaves the complementer at terminal point 11 (60Y11), and then enters package 63Y at point 22, flows through a diode, and becomes an output at terminal point 15 (63Y15). From point 63Y15 it enters an arithmetic shift-type core in package 61Y at point five (61Y5). This core also receives A-phase power pulses through terminal point 21 (61Y21) and B-phase blocking pulses through point 22 (61Y22). All other troubleshooting layouts follow this same pattern.

2.4 SHELF WIRING CHARTS

The shelf wiring charts show all package terminal points of the shelves and connections to and from each point. Each bay of the Processor contains eleven shelves -- A B C D E F G H J K L -- in the fixed bay and --M N P R S T V W X Y Z -- in the hinged bay. Each shelf has 100 package positions, and each shelf wiring chart shows wiring connections for 25 packages on one shelf. Figure 2-4 shows only four of these package positions.

Because the number of packages in a logical grouping varies, each wiring chart does not always show connections for one full logical group. For instance, the Register C package-group contains 39 packages, but only 25 appear on one chart. The remaining 14 are on another. The first four package positions of the Register C group are used for explanation of shelf wiring charts. These wiring charts include both internal and external wiring. Internal wiring is wiring within a logical group (not limited to a shelf), while external wiring is wiring between logical groups (not necessarily wiring between two shelves, as the logical groups may fall on one shelf). The wiring connectors and encircled connections on the example are shown for explanatory purposes only and refer to the section on Layout-to-Wiring charts.

The tabs at one edge of a package connector are numbered 1 to 22 on one side and 31 to 52 on the opposite side. Every terminal point shown on a troubleshooting layout is also shown on the wiring charts.

The packages receive power pulses, blocking pulses, d-c voltages, and ground connections from seven busbars below each shelf. Three volts d-c is carried on busbar 1, B-phase blocking pulses on busbar 2, A-phase power pulses on busbar 3, B-phase power pulses on busbar 5, A-phase blocking pulses on

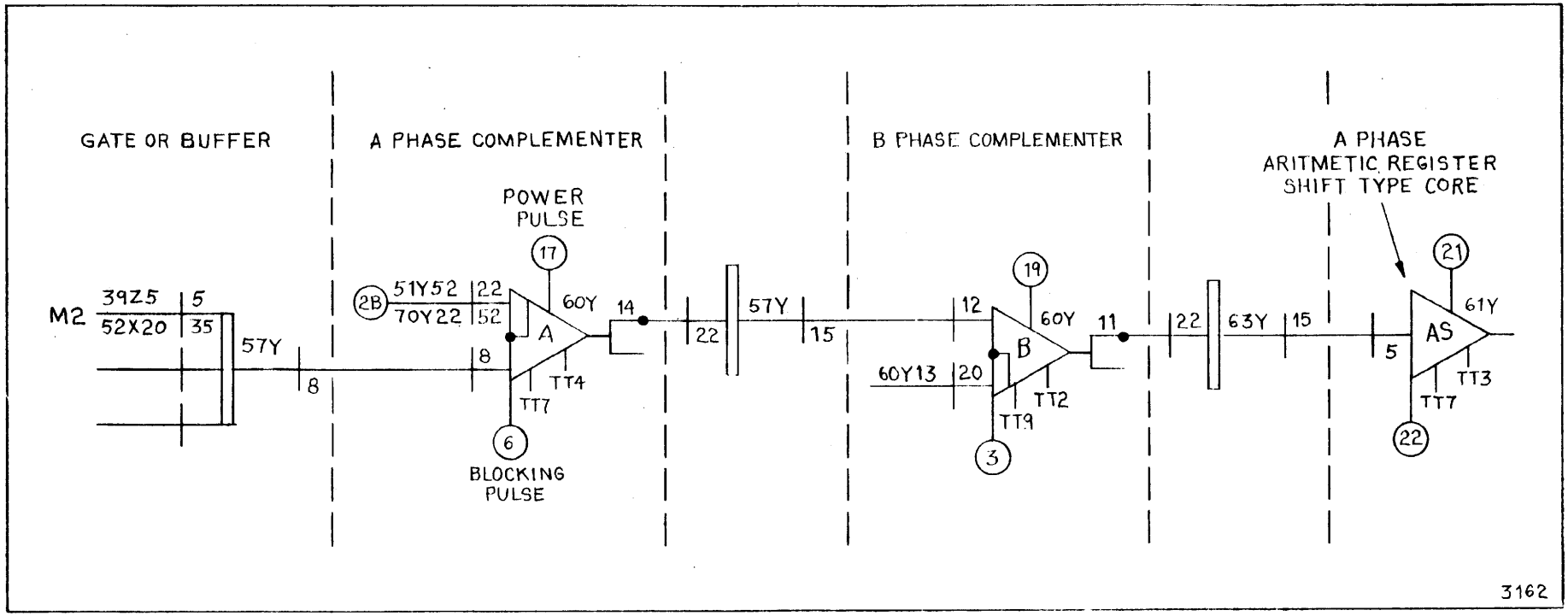


Figure 2-3 **Troubleshooting Layout Example**

busbar 6, and -29 volts d-c on busbar 7. Busbar 4 is a ground connection. All package contacts on the wiring chart with a Bus 1 through Bus 7 designation must be wired to the appropriate busbar.

Packages are numbered from 00 through 99 on each shelf, so that every package is designated by its position. Thus, package number 50 on shelf Y is package 50Y.

All shelf wiring in the Processor is color-coded according to its application. The following table shows the wiring color code used.

ABBREV.	COLOR	APPLICATION	BUS DESIGNATION
BRN	BROWN	+ VOLTAGE, +3	BUS 1
RED	RED	BLOCKING PULSE B	BUS 2
ORN	ORANGE	POWER PULSE A	BUS 3
YEL	YELLOW	GROUND	BUS 4
GRN	GREEN	POWER PULSE B	BUS 5
BLU	BLUE	BLOCKING PULSE A	BUS 6
VIO	VIOLET	- VOLTAGE, -29	BUS 7
BLK	BLACK	EXTERNAL WIRING	
WHT	WHITE	INTERNAL WIRING	
CLR	CLEAR	FUNCTION SIGNALS + TIMING SIGNALS	
GRY	GREY		

TABLE 2-1 UCT COLOR CODE

A typical example of package wiring is package number 52 on the Y shelf, or 52Y (Figure 2-4). Terminal point 52Y1 is the first point on the left side of the package 52Y; it connects to busbar 6, which carries the A-phase blocking pulses. The letters BLU alongside point 52Y1 indicate that a blue wire is used to connect this tab to busbar 6. Terminal point 53Y3, tab 3 of package 53 on the Y shelf, is connected to busbar 2, which carries B-phase blocking pulses, by a red wire. Tab connections which have no representation on the wiring layout are not used, so that point 52Y31 (blank space) is a package tab which is

not connected. Terminal point number 50Y12 is connected by a white wire to tab 10 on package 51Y (51Y10). Terminal 52Y37 is connected with a white wire to 52Y42. The lettering AR1-S across package 52Y indicates that it is an Arithmetic Register Package. The package type is always shown in the location of its key. Thus, all AR1-S packages are marked at point 3, 33 on the wiring charts.

2.5 SIGNAL FLOW AND WIRING CONNECTIONS

Figure 2-4 is the wiring chart for the layout diagram shown in Figure 2-5. The following table details the relationship between these two diagrams.

SIGNAL FLOW Refer to Fig. 2-5	CONNECTIONS Refer to Fig. 2-4
Signal RSC from 08X48 enters package 50Y at point 1.	A black wire connects 08X48 with tab 50Y*.
The signal RSC is sent from 50Y1 through a diode in package 50Y to 50Y9.	Two leads on package connect point 1 to diode and diode to point 9*.
The signal also leaves package 50Y at point 31 and enters package 63Y at point 1.	A black wire connects 60Y31 to 63Y1*.
From 50Y9 the signal enters package 53Y at point 10.	A white wire connects 50Y to tab 53Y10.
A signal from 51Y45 enters package 53Y at point 18.	A white wire connects 51Y45 to 53Y18.
The two signals then enter a complementer in package 53Y.	A lead on package connects points 53Y18 and 53Y10 to complementer.
A B-phase Power pulse enters complementer 53Y at point 21.	A green wire connects busbar 5 to tab 53Y21.
An A-phase blocking pulse enters complementer 53Y at point 4.	A blue wire connects busbar 6 to 53Y4.
The signal is sent from the complementer to 53Y13.	A lead on package connects complementer 53Y to tab 53Y13.
From 53Y13 the signal enters package 50Y at point 5.	A white wire connects 53Y13 with 50Y5.

*The wiring between these two points is not shown because the figure being used does not contain both ends of the connection.

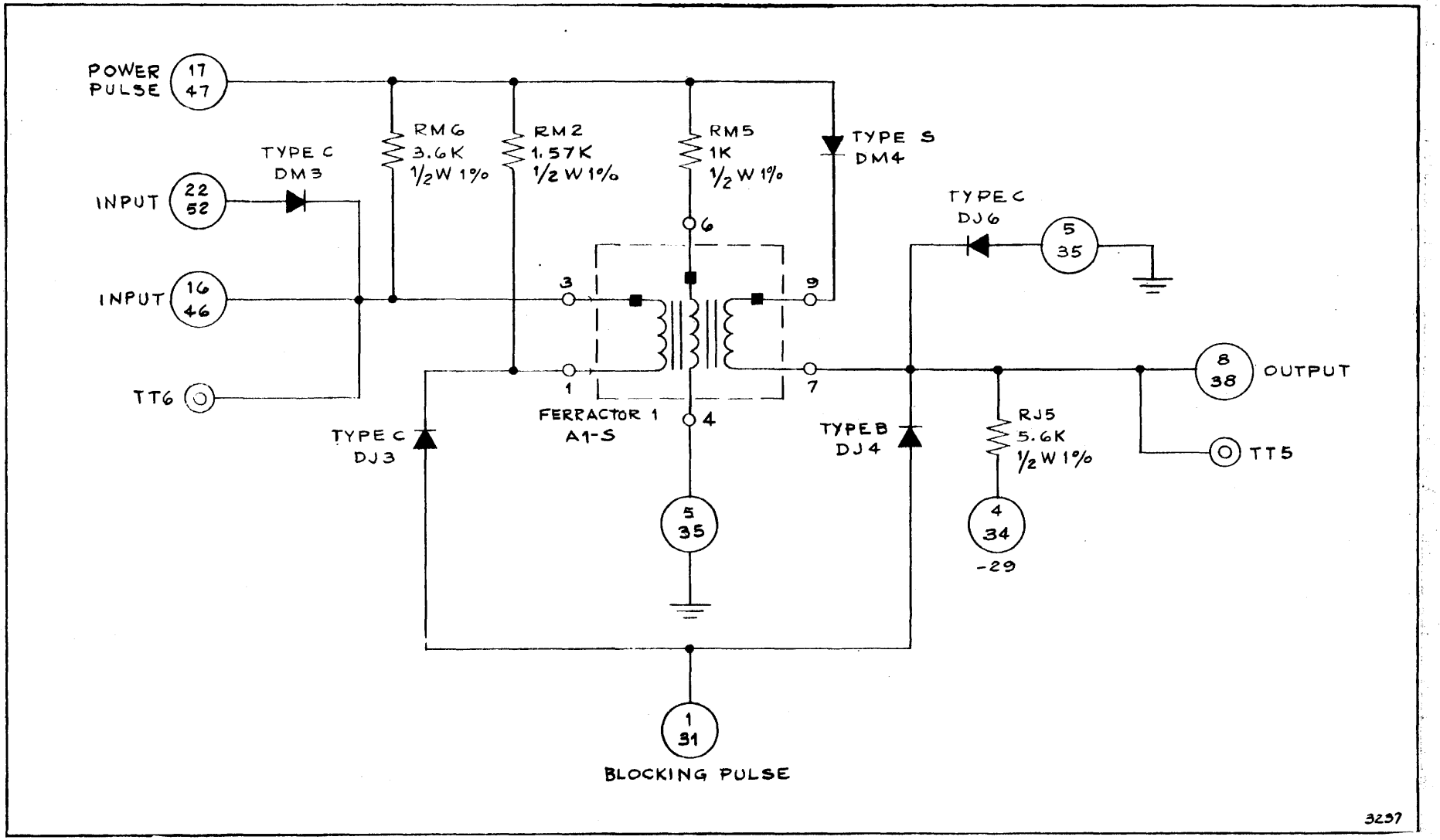


Figure 2-6 Package Schematic Example

SIGNAL FLOW	CONNECTIONS
Signal L10D comes from 33Z41 and enters package 50Y at point 6.	A black wire connects 33Z41 with 50Y6*.
Signal A10D comes from 91V13 and enters package 50Y at point 37.	A black wire connects 91V13 to 50Y37*.
These three signals are then sent through a diode in package 50Y and the resultant signal output goes to terminal point 50Y8.	Three leads on the package connect the diode to 50Y8.
The signal then leaves the package 50Y at point 8 and enters package 53Y at point 7.	A white wire connects 50Y8 to 53Y7.
Signal X10D coming from terminal point 77TII enters package 53Y at point 46.	A black wire connects 77TII to 53Y46*.
These two signals are sent to a complementer in package 53Y.	A lead on the package connects terminal points 53Y7 and 53Y6 to complementer.
An A-phase power pulse enters the complementer from 53Y17.	An orange wire connects tab 53Y17 to busbar 3.
A B-phase blocking pulse enters the complementer 53Y at point 6.	A red wire connects busbar 2 to 53Y6.
The resultant output signal RD1 then flows from the complementer to 53Y15.	A lead on package connects the complementer 53Y to point 15.
Signal RD1 then leaves the package at 53Y15 and enters package 10Z at point 15.	A black wire connects 53Y15 to 10Z15*.

*The wiring between these two points is not shown because the figure being used does not contain both ends of the connection.

2.6 PACKAGE SCHEMATICS AND PICTORIALS

There is a schematic and pictorial for each type of package used in the UCT. Each schematic shows the complete circuitry of a package with circuit components named according to the position they occupy on the package board.

Figure 2-6 is a sample schematic of the non-complementing single power amplifier package, which is shown in Figure 2-2 in the logic and

troubleshooting diagram representation. The package pictorial drawing of this circuit, Figure 1-11, shows the circuit components mounted in position on the board.

The input and output terminals (Section 1.3.1) of the package used in this circuit are circled and labeled. Example: the inputs to this circuit are terminal points 22, 52 and 16, 46. The two terminals (22, 52) that make up a pair are bifurcated as explained in Section 1.3.1.

The power pulse to this amplifier enters the circuit at terminal point 17, 47, the blocking pulse at 1, 31, -29V at 4, 34, and terminal point 5, 35 is connected to ground. The circled single numbers represent the pin numbers of the magnetic cores.

The circuit components are all labeled on the schematic according to their locations on the board. Resistor RM6 is mounted in row M, position 6, diode DJ3 is mounted in row J, position 3 (Figure 1-11). Section 1.3.1 explains the addressing of circuit components. TT5 and TT6 are test terminals for the output and input signals.

2.7 MOUNTING BOARDS AND ADDRESSING SYSTEM

Circuit components on a mounting board are named on the circuit schematic according to their address on the board. There are three types of mounting boards. One type of board has three rows of numbered mounting positions labeled M, L and N (top to bottom) and a second type of board has three rows labeled J, H, and K (top to bottom). On these two types, the address consists of the initial letter of the component (R for resistors, D for diode, C for capacitor, etc.), a letter designating the row, and the number of the specific mounting position in the row. Thus, a diode mounted on position 3 of row J is DJ3.

When a component is mounted between row J and either row H or K, the address is given for the J row. If a component is mounted between rows H and K, the K row is used in the component address. On the L-M-N type boards, a component mounted between row M and either row L or N, is given an M-row address. If the component is mounted between rows L and N, the N row is used in the component address. Rows L and H (middle rows of the two types of mounting boards) are never used in the address of a component unless all leads of a component are connected to that row. For example, if the three leads of a transistor were connected to mounting positions 18, 20, and 22 of row H, its address would be QH18. The mounting position used in the address is the one to which the transistor base is connected. Engineering Drawing DX808, 080 illustrates these two types of mounting boards. The circuit schematics indicate which mounting boards are involved in the circuit. Mounting boards are abbreviated to the letters MB and a number on all schematics and wiring drawings except on Read-Punch drawings where the letters TB are used.

The third type of mounting board has two rows of mounting positions. The positions are numbered continuously through the two rows. For example, if each

SHELF
Y

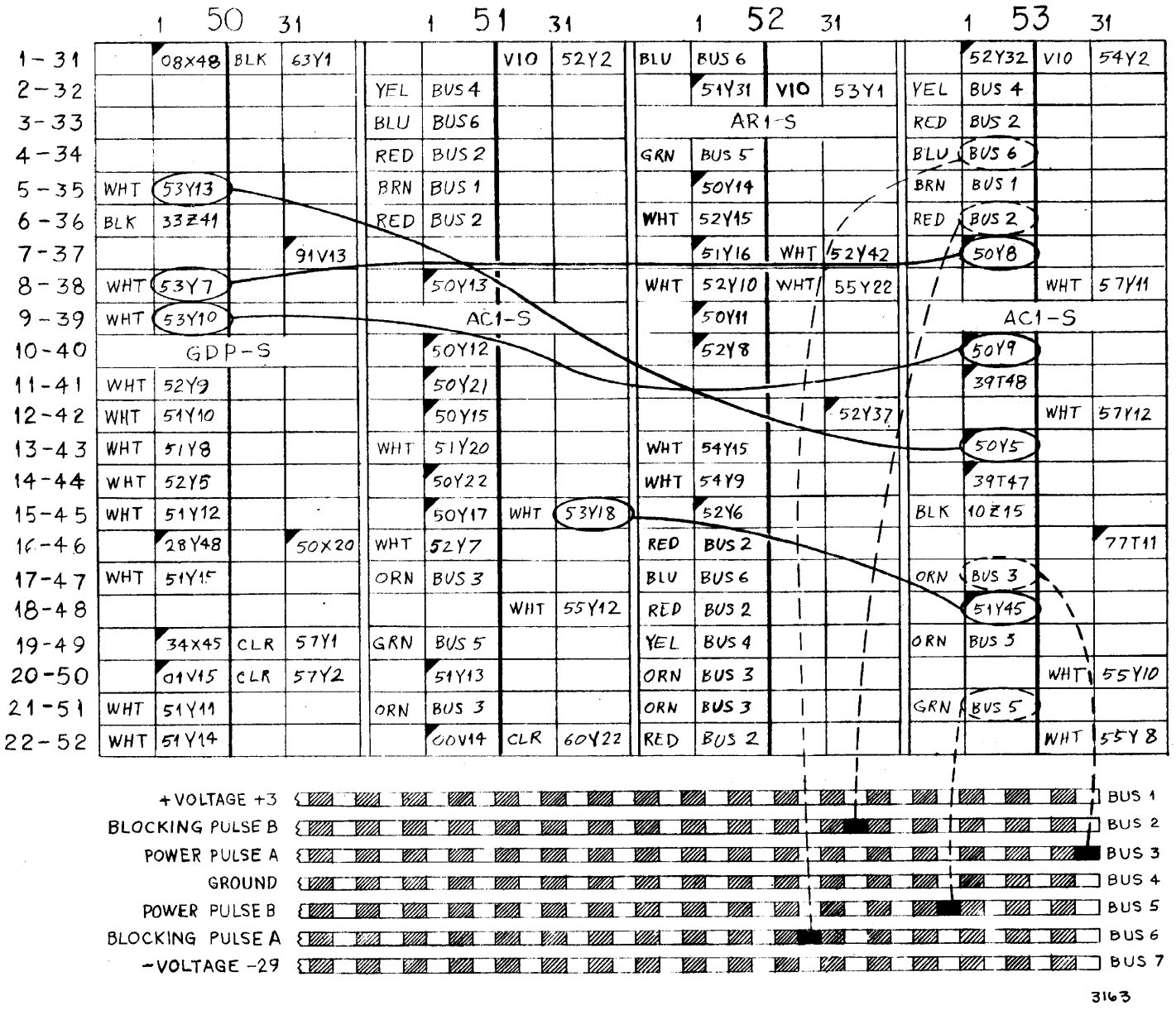


Figure 2-4 Shelf Wiring Chart

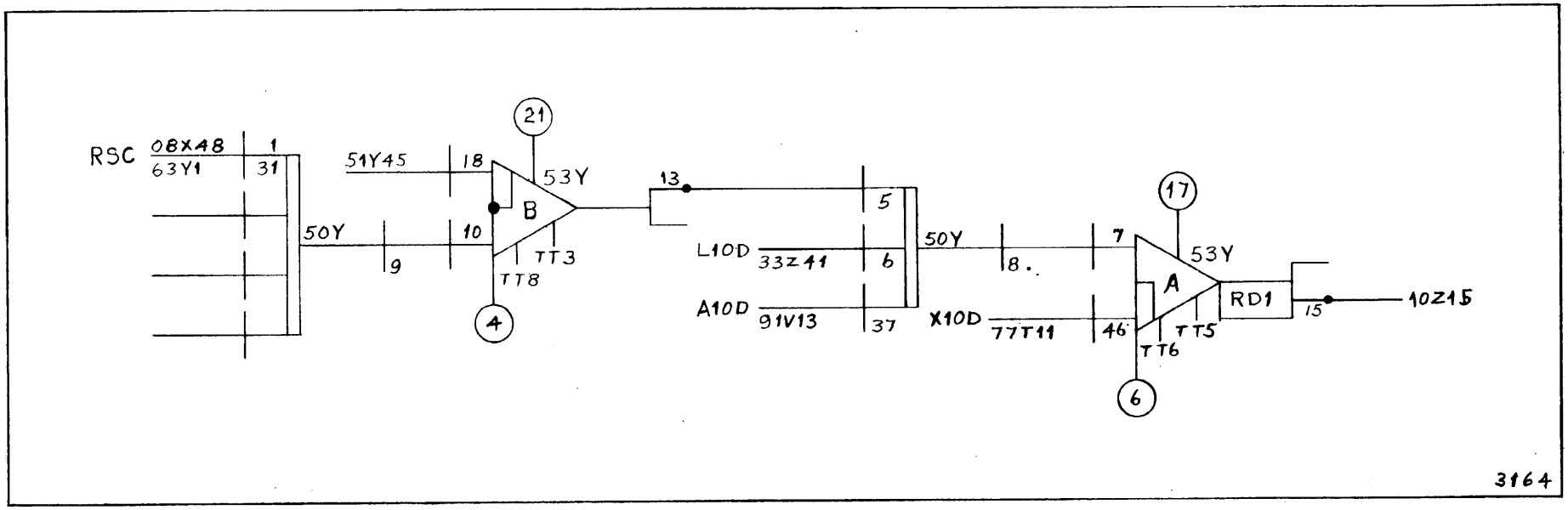


Figure 2-5 Signal Flow Example

row has 12 mounting positions, the first row is numbered 1 to 12 and the second row 13 to 24. The address of a circuit component mounted on this type of board consists of the initial letter of the component, the number of the mounting board, and the lowest position number the component is mounted on. Thus, if a diode is mounted between position 2 and 14 of mounting board 6, its address would be DMB6-2. In some cases mounting boards of this type are identified by a letter instead of a number. If the diode in the previous example was on mounting board A, its address would be DA2. This type of mounting board is shown on Engineering Drawing DX601, 083.

SECTION THREE

CONTROL PANELS

3.1 GENERAL

All controls and indicators for the processor are contained in the Engineers and Operators Panels. The purpose of this section is to provide an explanation of the function of each control and indicator on the panels.

This section will explain only the panels on the processor. The Read-Punch, Printer, and Card Reader Manuals each contain an explanation of their respective panels.

3.2 ENGINEERS PANEL

The Engineers Panel (Figure 3-1) located on the processor is intended primarily for the use of technicians and maintenance men. The panel contains 12 indicator lights, three illuminated pushbutton switches, a voltmeter, voltage monitor switch, and a polarity switch for the voltmeter. All indicators on this panel have clear glass domes above the neon lamps, which glow orange when lit. The function of each light and/or switch is explained in the following paragraphs.

3.2.1 Pushbuttons and Indicators

DOOR INTERLOCK - lights when the door interlock switch is open, indicating that the processor bays are open.

AIR FLOW - lights whenever the air circulation falls from the desired rate of flow in the processor.

OVERHEAT - lights to indicate the temperature has gone above the desired limit in the processor.

DRUM - lights to indicate either of two off-normal conditions of the drum: (1) that the drum temperature has risen above the desired limit or; (2) the spacing between the heads and drum has become less than or greater than the required distance. Either condition energizes a relay to turn off power and light the DRUM indicator. The relay is reset by depressing the FAULT RESET/FUSE TEST pushbutton.

CYCLING UNIT - lights when an error is detected in the cycling unit indicating that the timing band sentinels have occurred at the wrong time or in the wrong phase or that the series circuit is open.

PRINTER CODE WHEEL - lights to indicate a parity error in reading from the code generator.

MAIN STORAGE - lights to indicate parity error when reading from the main storage drum.

ADDRESS STORAGE - lights to indicate a parity error when reading from the TS band.

PRINT BUFFER STORAGE - lights to indicate a parity error when reading from the Print Buffer Band.

DELETE STOP - lights when depressed to over ride all errors, instruction and control, that would normally stop the computer. This pushbutton remains locked allowing the computer to override all errors until it is depressed a second time (alternate-action).

MUL/DIV TEST - lights when depressed to stop processor when it is executing a multiply or divide instruction. This button must be depressed a second time to allow the processor to continue (alternate-action).

FAULT RESET/FUSE TEST - depress to test for blown fuse in processor and/or printer. If there is a blown fuse in either or both units, the PRINTER FUSE and/or PROCESSOR FUSE indicator will light. Depress to reset overload relay of +3 volt and -1.5 volt circuits and to reset the drum overheat and drum head spacing relays (momentary).

OVERLOAD RELAY - lights to indicate a current overload on the +3 volt and -1.5 volt circuits.

3.2.2 Voltage Monitor

VOLTAGE MONITOR METER - indicates percent deviation from normal voltage level.

POLARITY SWITCH - set to polarity of voltage being monitored.

VOLTAGE MONITOR SWITCH - set to voltage level that is to be monitored. Table 3-1 lists the switch positions and the voltage that is monitored for each position.

TABLE 3-1

Polarity Switch Set on Plus

POSITION	VOLTAGE	MEASURED TO
A	+ 3	GND
B		
C	+ 6	GND
D	+10	GND
E	+16	GND
F	+18	+19
G	+19	+16
H	+20	+19
J	+28.5	+30
K	+30	+35
L	+35	GND
M	+45	GND
N	+100	GND
P	+150	+100
R	+300	GND
S		
T		
V	Clock A	GND
W	Clock B	GND
OFF		

TABLE 3-1 (Continued)

Polarity Switch Set on Minus

POSITION	VOLTAGE	MEASURED TO
A	-1.5	GND
B		
C		
D	-10	GND
E	-11.5	-10
F		
G		
H		
J	-29	GND
K	-30 or -40	GND
L	-32 or -42	-30 or -40
M	-45 or -55	-30 or -40
N	-50	-29
P	-150	GND
R		
S		
T		
V		
W		
OFF		

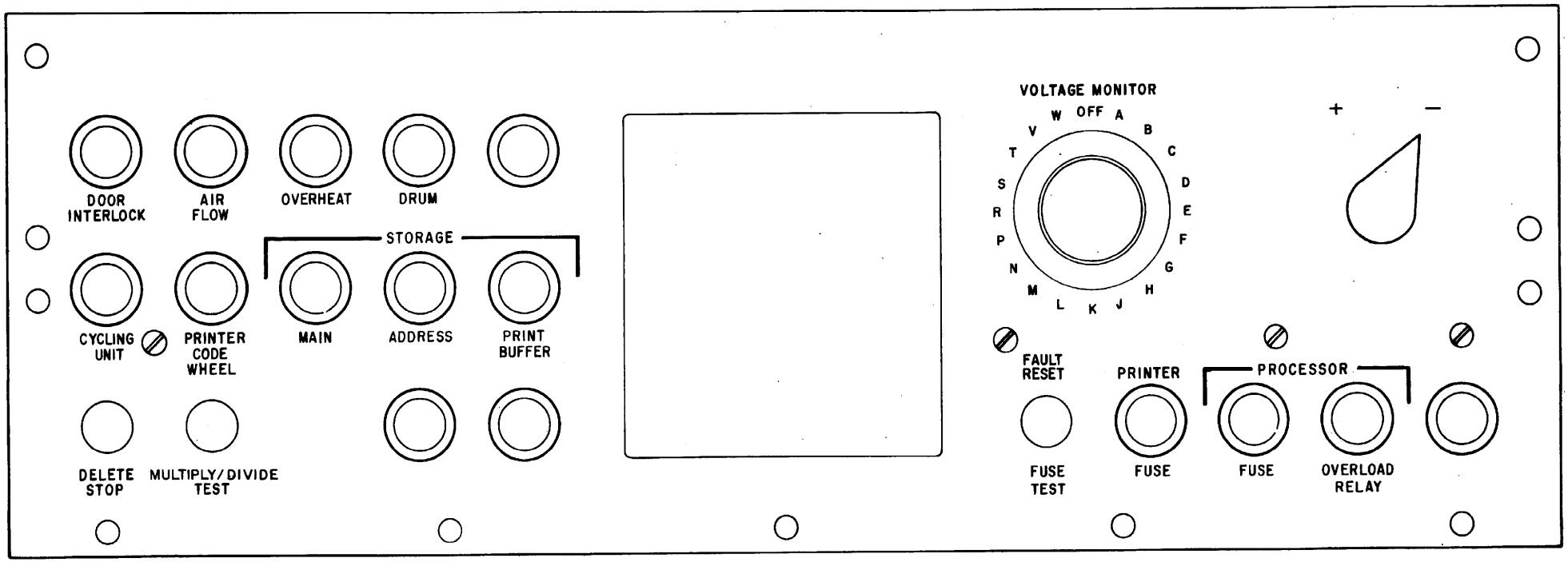


Figure 3-1 Engineers Panel

3.3 OPERATORS PANEL

The operators panel (Figure 3-2) is the main control panel of the computer. It contains most of the controls and indicators necessary to operate the computer. Each pushbutton and indicator is described in the following paragraphs.

STATIC REGISTER - 8 lights to indicate the contents of the Static Register. The number in the lights indicate the weight of each bit.

REGISTER SELECTOR - four illuminated pushbuttons, L, X, A, C, used to select register to be displayed by the REGISTER CONTENTS lights. The four pushbuttons are interlocked to prevent selection of more than one register (alternate action).

SIGN - two lights to indicate the sign of the contents of the register being displayed.

REGISTER CONTENTS - 40 lights indicating the contents of any one of the four registers, A, X, L and C.

PRINTER OFF NORMAL - lights red when an abnormal condition occurs in the printer or when the printer is not prepared to print. Refer to lights on the Printer panel for cause.

CARD READER OFF NORMAL - lights red when an abnormal condition occurs in the Card Reader. Refer to lights on the Card Reader panel for cause.

READ PUNCH OFF NORMAL - lights red when an abnormal condition occurs in the Read-Punch or when the Read-Punch motor is not running. Refer to lights on the Read-Punch panel for cause.

PROCESSOR OFF NORMAL - lights red when a malfunction occurs in the Processor, when the stop switch is depressed, or if the processor is operated in a non-continuous mode. Refer to the lights on the Engineers panel for cause.

D.C. - lights green when dc is on. Depress to turn dc off (momentary).

A.C. - lights amber when the DC READY pushbutton is depressed to indicate ac is on. Depress to turn ac and dc off (momentary).

DRUM - lights when DC READY is depressed to indicate drum is on. Depress to stop drum revolution (momentary).

D.C. READY - lights amber when drum is at full speed and AC time delay has expired. Depress to turn ac and drum on and depress when lit to

turn dc on (momentary).

96 CHECK - depress to inhibit operation of buffer transfer check circuit. Lights white when activated (alternate action). (Not shown on Figure 3-2).

ALERT 96 CHECK - lights to indicate that a buffer transfer was missed on a 96 instruction. (Not shown on Figure 3-2).

READ PUNCH - EMPTY STATION INHIBIT - depress to cause the computer to continue even though one or more stations are empty in the Read-Punch unit. Lights amber when activated (momentary).

READ PUNCH-NO PUNCH - depress to eliminate punching in the Read-Punch Unit. Lights amber when activated. Must be depressed a second time to be released and allow punching (alternate action).

NEXT ADDRESS m - when lit, indicates next memory search will be for the m address. When not lit and m address is desired, depress to transfer control from c to m (momentary).

NEXT ADDRESS c - when lit, indicates next memory search will be for c address. When not lit and c address is desired, depress to transfer control from m to c (momentary).

GENERAL CLEAR - depress to clear controls, indicators, and flip-flops. Lights red when activated (momentary).

PRINTER - NO PRINT - eliminates printing when depressed. Lights amber when activated. Must be depressed a second time to be released and allow printing (alternate action).

PRINTER-ONE LINE PRINT - when this pushbutton is depressed, the processor proceeds normally until the next print instruction is staticized and then stops. Lights when activated (alternate action).

READ PUNCH - ONE CARD R. P. U. - when this pushbutton is depressed the processor proceeds normally until the next card feed instruction is staticized and then stops. Lights when activated (alternate action).

READER-ONE CARD READER - when this pushbutton is depressed the processor proceeds normally until the next card feed instruction is staticized, then stops. Lights when activated (alternate action).

COMPARISON STOP - when this pushbutton is depressed the processor completes the next comparison instruction, then stops. Lights when activated (alternate action).

ONE INSTRUCTION - when this pushbutton is depressed, the processor staticizes the next instruction and stops. Lights when activated (alternate action).

CONTINUOUS - when this pushbutton is depressed the processor proceeds on a continuous basis. Lights green when activated. This pushbutton and the five other pushbuttons under the heading OPERATION in Figure 3-2 are all interlocked. Only one can be activated at one time. When any one is depressed, it releases the pushbutton previously depressed (alternate action).

COMPUTATION RUN - depress to start computation. Lights green when activated (momentary).

COMPUTATION STOP - depress to stop computation. Lights amber when activated (momentary).

3.4 KEYBOARD

The keyboard (Figure 3-3) contains 13 pushbuttons and is used to type a manual entry into the computer. The manual entries are sent to the register selected by depressing one of the four REGISTER SELECTOR pushbuttons on the operators panel.

A - Keyboard alert - depressed to activate keyboard.

Keyboard Ready - lights white when keyboard is activated.

0-9 Keys - used to type words into the computer.

+ and - keys - releases typed word into selected register and disconnects keyboard.

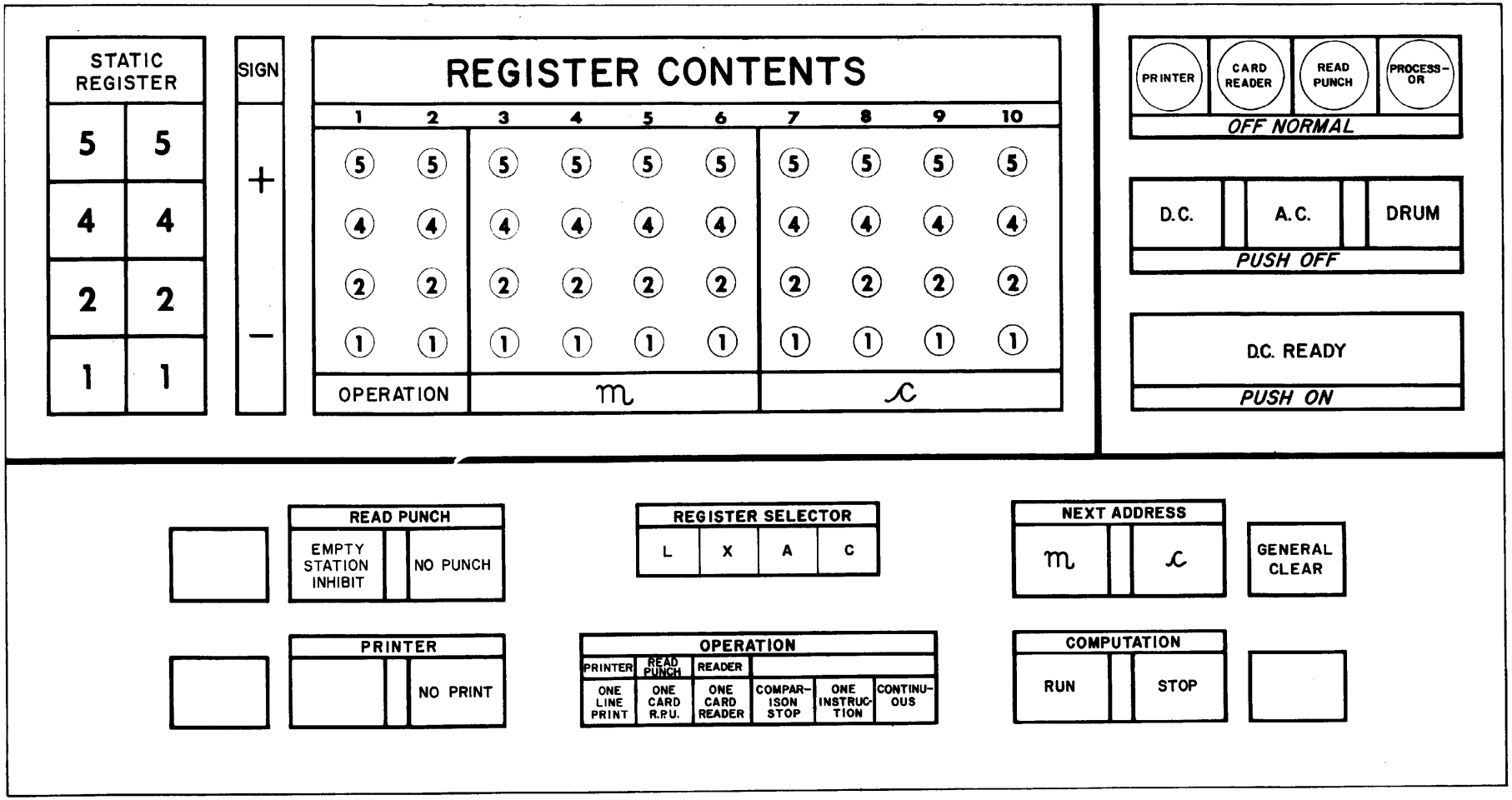


Figure 3-2 Operators Panel

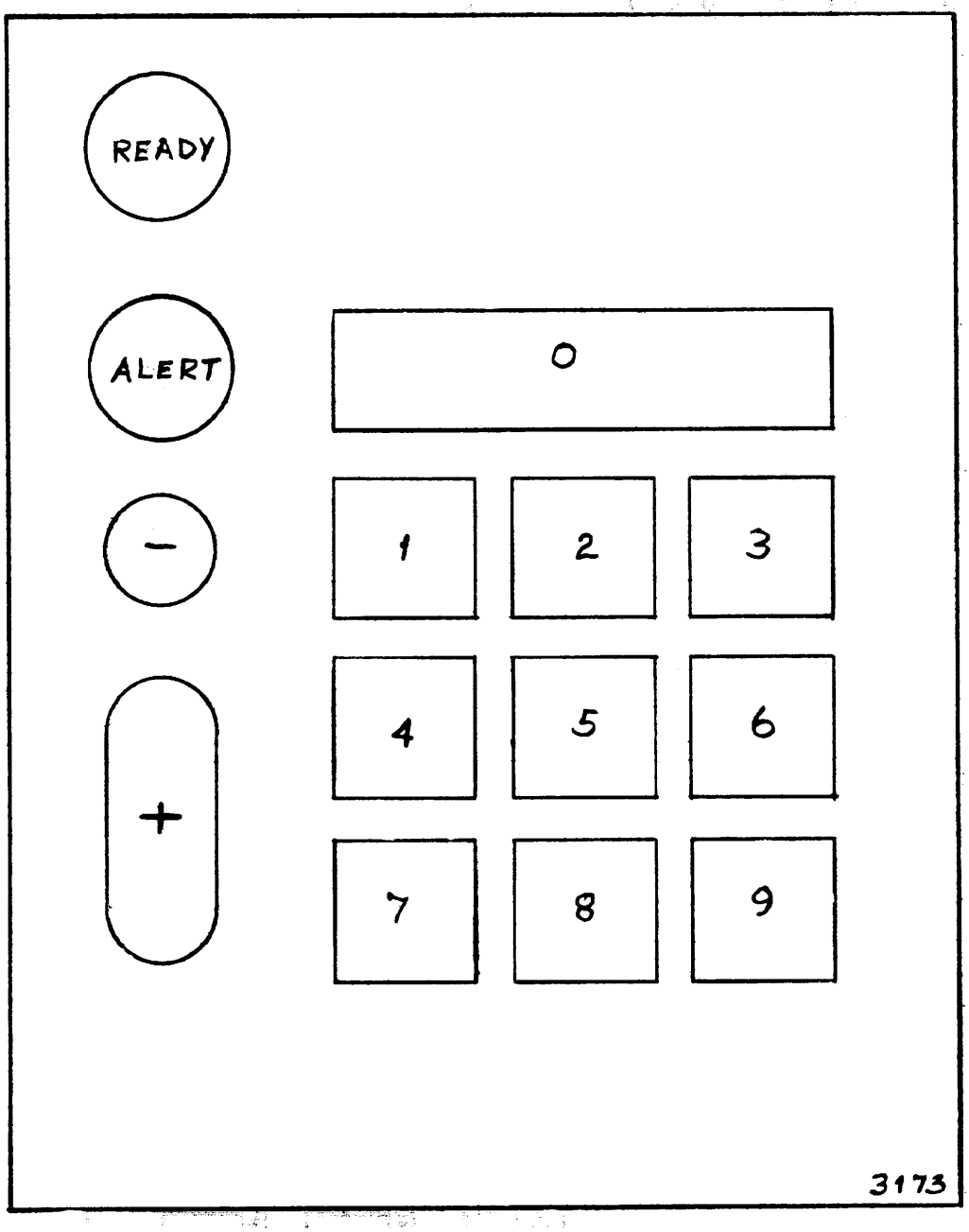


Figure 3-3 Keyboard

APPENDIX

TABLE A-1

UCT PROCESSOR RELAYS

RELAY NO.	LOCATION	NAME	ENGINEERING DRAWINGS
Relay 3	Figure 1-6, 5	Blower Holdover	Primary Power Control
Relay 4	Figure 1-3, 12	Blower Contactor	P1 and P2 - AC Power Distribution Coil - Primary Power Control
Relay 5	Figure 1-6, 19	Air Flow	Primary Power Control
Relay 6	Figure 1-3, 11	Drum Contactor	P1 - AC Power Distribution Coil, P2, P3 - Primary Power Control
Relay 7	Figure 1-7, 10	Drum Relay	Primary Power Control
Relay 8	Figure 1-6, 13	Drum Ready	
Relay 9	Figure 1-7, 11	DC Relay	Primary Power Control
Relay 10	Figure 1-6, 12	DC Ready	Primary Power Control
Relay 11	Figure 1-3, 10	AC Contactor	P1 and P2 - AC Power Distribution Coil and P3 - Primary Power Control
Relay 12	Figure 1-3, 9	DC Contactor	P1, P2, P3, and P4 - AC Power Distribution Coil and P5 - Primary Power Control
Relay 13	Figure 1-6, 4	AC Fault	Fuse Alarm Circuit
Relay 14	Figure 1-6, 3	DC Fault	Fuse Alarm Circuit
Relay 15	Figure 1-6, 17	Standby Fuse Alarm	Pole - Primary Power Control Coil - Fuse Alarm Circuit
Relay 16	Figure 1-6, 16	AC Alarm	Fuse Alarm Circuit

TABLE A-1 (Continued)

RELAY NO.	LOCATION	NAME	ENGINEERING DRAWINGS
Relay 17	Figure 1-6, 15	+ DC Alarm	P1 - Primary Power Control Coil-Fuse Alarm Circuits
Relay 18	Figure 1-6, 14	- DC Alarm	P1 - Primary Power Control Coil-Fuse Alarm Circuit
Relay 19	Figure 1-6, 11	General Clear	Cycling Unit
Relay 20	Figure 1-6, 19	Processor Off Normal	Off Normal Indicators
Relay 21	Figure 1-6, 20	High Speed Printer Off Normal	Off Normal Indicators
Relay 22	Figure 1-6, 21	Read-Punch Off Normal	Off Normal Indicators
Relay 23	Figure 1-6, 1	Card Reader Off Normal	Off Normal Indicators
Relay 24	Figure 1-6, 10	Start	Interrupted Operation
Relay 25	Figure 1-7, 8	Overcurrent +3V	Coil - DC Power Distribution P1 - Off Normal Indicators
Relay 26	Figure 1-7, 7	Overcurrent + 3V	Coil - DC Power Distribution P1 - Off Normal Indicators
Relay 27	Power Control Tray	Overcurrent -1.5V	Coil - DC Power Distribution P1 - Off Normal Indicators

TABLE A-1 (Continued)

RELAY NO.	LOCATION	NAME	ENGINEERING DRAWINGS
Relay 28	Figure 1-6, 2	Input Ready	Interrupted Operation
Relay 29	Figure 1-6, 7	PS Short Circuit	Off Normal Indicators
Relay 30	Figure 1-6, 6	Memory Write Inhibit	Coil - Primary Power Control P1, P3, P4 - DC Power Distribution
Relay 31	Bleeder Resistor Panel	Meter Relay	Primary Power Control
Relay 32	Figure 1-6, 8	Clock Alarm	Primary Power Control
Relay 33	Figure 1-6, 9	Drum Alarm	Primary Power Control
Relay 34	Figure 1-7, 4	Drum Motor Start	AC Power Distribution
Relay 35		Drum Speed Control	Primary Power Control
Relay 36	Power Control Tray	Drum Air Flow	Primary Power Control
Relay 37	Power Control Tray	General Air Flow	Primary Power Control

TABLE A-2

UCT PROCESSOR BARRIER STRIPS

NUMBER	LOCATION	DISTRIBUTION OF	ENGINEERING DRAWING
BS1	Figure 1-2, item 12	Primary input power	AC Power Distribution Primary Power Control
BS2	Figure 1-2, item 8	Automatic Start Clock Input	Primary Power Control
BS4		A. C. N.	AC Power Distribution
BS5		A. C. N.	AC Power Distribution
BS10	Figure 1-2, item 5	-1.5V DC	DC Power Distribution
BS11	Figure 1-2, item 5	-10V DC	DC Power Distribution
BS12	Figure 1-8, item 14	+3V and -29V DC	DC Power Distribution
BS14	Figure 1-2, item 5	-30V, -32V, and -45V DC	DC Power Distribution
BS16	Figure 1-8, item 13	+3V and -29V DC	DC Power Distribution
BS18	Figure 1-2, item 5	-50V, +6V, +4.75V, and +10V DC	DC Power Distribution
BS19	Figure 1-2, item 5	+16V and +20V DC	DC Power Distribution
BS20	Figure 1-2, item 5	+35V, +28.5V, +19V, +18V and +30V DC	DC Power Distribution
BS22	Figure 1-2, item 5	+45V DC, Ø A and Ø B	DC Power Distribution Voltage Monitor
BS23		+3V DC	
BS24			

TABLE A-2 (Continued)

NUMBER	LOCATION	DISTRIBUTION OF	ENGINEERING DRAWING
BS25			
BS26			
BS27			
BS30	Figure 1-2, item 18	+3V, +16V, and +10V DC	DC Power Distribution
BS31	Figure 1-2, item 17	+45V, +100V, and +300V DC	DC Power Distribution
BS32	Figure 1-2, item 16	-1.5V, -29V, and -150V DC	DC Power Distribution
BS33	Figure 1-7, item 9	Over current relay connector	OFF Normal Indicator
BS34	Figure 1-2, item 15	Miscellaneous to area units	
BS35	Figure 1-8, item 13	+3V and -29V DC	DC Power Distribution
BS36	Figure 1-8, item 14	+3V and -29V DC	DC Power Distribution
BS37	Figure 1-2, item 14	Motor Barrier Strip	AC Power Distribution
BS38	Figure 1-8, item 14	Miscellaneous	OFF Normal Indicators
BS39	Figure 1-8, item 13	Miscellaneous	OFF Normal Indicators
BS40	Figure 1-7, item 1	+45V Power Supply (Sola)	
BS41	Figure 1-2, item 25	+300V Supply (Sola)	
BS42	Figure 1-2, item 22	-30V, -48V Supply (Sola)	
BS43	Figure 1-2, item 19	-150V Supply (Sola)	

TABLE A-2 (Continued)

NUMBER	LOCATION	DISTRIBUTION OF	ENGINEERING DRAWING
BS44	Figure 1-2, item 1	-800V Supply (Sola)	
BS45	Figure 1-2, item 28	-29V Supply (Sola)	
BS46	Figure 1-3, item 3	+100V Supply (Sola)	
BS47	Figure 1-3, item 4	+3V Supply (Sola)	
BS48	Figure 1-3, item 5	+16V Supply (Sola)	
BS49	Figure 1-3, item 6	+2V (-32V, -50V) Supply (Sola)	
BS50	Figure 1-3, item 7	+6V Supply (Sola)	
BS51	Figure 1-2, item 27	+15V (-45V, -63V) Supply (Sola)	
BS52	Figure 1-2, item 26	+35V Supply (Sola)	
BS53	Figure 1-2, item 24	-50V (-1650V) Supply (Sola)	
BS54	Figure 1-2, item 23	+300V (-1300V) Supply (Sola)	
BS55	Figure 1-2, item 21	-10V Supply (Sola)	
BS56	Figure 1-2, item 20	-1.5V Supply (Sola)	
BS57	Figure 1-3, item 1	-800V Supply (Sola)	
BS60		Ground	
BS61		Ground	
BS63		Alternator and Clock Blower	AC Power Distribution
BS64		Alternator Drove Motor	AC Power Distribution

TABLE A-2 (Continued)

NUMBER	LOCATION	DISTRIBUTION OF	ENGINEERING DRAWING
BS65		Drum Blower	AC Power Distribution
BS66		Thermo couples on Drum Blower	Primary Power Control
BS67		Clock Output	
BS68	Clock Driver Chassis		
BS70			
BS71			
BS72			
BS73			
BS74			
BS75			
BS76			
BS77			
BS78			
BS79			
BS80	Meter Panel		
BS81	Meter Panel		
BS82	Meter Panel		
BS83	Meter Panel		

TABLE A-3

UCT PROCESSOR SELENIUM RECTIFIERS

RECTIFIER NO.	LOCATION	USE	ENGINEERING DRAWING
SR1	Figure 1-5, 10	Interlock OFF Normal Circuit	OFF Normal Indicators
SR2	Figure 1-5, 10	Air Temperature OFF Normal Circuit	OFF Normal Indicators
SR3	Figure 1-5, 10	Air Flow OFF Normal Circuit	OFF Normal Indicator
SR4	Figure 1-5, 10	Fuse Fault Circuit	Fuse Alarm Circuit
SR5	Figure 1-5, 10	Fuse Fault Circuit	Fuse Alarm Circuit
SR6	Figure 1-5, 10	HSP Fuse Fault Circuit	Fuse Alarm Circuit
SR7	Figure 1-5, 10		Fuse Alarm Circuit
SR8	Figure 1-5, 10	Standby and AC Fault RLY Circuits	Processor Fuseboards
SR9	Figure 1-5, 11	Standby and AC Fault RLY Circuit	Processor Fuseboards
SR10	Figure 1-5, 11	Standby and AC Fault RLY Circuit	Processor Fuseboards
SR11	Figure 1-5, 11	Standby and AC Fault RLY Circuit	Processor Fuseboards
SR12	Figure 1-5, 11	Standby and AC Fault RLY Circuit	Processor Fuseboards
SR13	Figure 1-5, 11	Standby and AC Fault RLY Circuit	Processor Fuseboards
SR15	Figure 1-5, 11	Overcurrent Circuit	OFF Normal Indicators
SR16	Figure 1-5, 11	Drum Alarm Circuit	Primary Power Control